Investigation of A Novel Single Carrier Based Space Vector Pulse Width Modulation Techniques for Cascaded Multi level Inverter fed Induction Motor Drive*

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Abstract. In recent days the pulse width modulation plays an important role in the modeling and control of multi-level inverters in order to obtain a low harmonic distortion of output voltage and current, reduced EMI and maximum number of output voltage levels. In this paper a novel single carrier PWM techniques is presented for Cascaded H-bridge multi level inverter fed induction motor drive. In this the performance of proposed drive is investigated for Total harmonic distortion, torque ripples, speed, line currents, phase voltages and line voltages by simulating the single carrier PWM technique at low frequency. This novel single carrier PWMs generated by injecting a suitable offset magnitude to reference sine modulation will resemble the SVPWM like performance for effective utilization of the DC-link voltages. It is shown that the magnitude of fundamental output voltage is enhanced like SVPWM technique from FFT analysis. This modulation strategy is analyzed for five-level, seven level, nine level and eleven level Cascaded H-bridge Multi level Inverter topology. The proposed inverter topology and control strategies are simulated using MATLAB/SIMULINK software. This novel single carrier PWM techniques can be applied to N-level cascaded H-bridge multi level inverter.

Keywords: single carrier PWM, single carrier based conventional SVPWM, cascaded h-bridge MLI, induction motor, THD

1 Introduction

The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. The unipolar PWM are the most preferred pwm control techniques. Even though space vector modulation (SVM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation. The operation theory will be discussed with the aspect of Unipolar PWM[13]. Several multicarrier techniques have developed to reduce the distortion in multilevel inverter, based on the classical SPWM with triangular carriers, some methods use carrier disposition and others use phase shifting of multiple carrier signals[5]. Multilevel inverter structures have been developed to overcome shortcomings in solid-state switching device ratings so they can be applied to higher voltage systems. The multilevel voltage source inverters[11].

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. Multilevel inverters as the name indicates produce more than two levels at its output phases. The multilevel inverters also provide benefits like improvement in output voltage spectrum etc. The multilevel inverters with neutral point clamped (NPC) or diode clamped technology were introduced

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during 1980. In 1990s, new multilevel inverters topologies were introduced. Some important multilevel inverter topologies are neutral point clamped, H-bridge and flying-capacitor type. However, due to simple construction features and other advantages, the neutral point clamped topology is widely used. Multilevel inverters offer many benefits for higher power applications. In particular, these include an ability to synthesize voltage waveform with lower harmonic content than two-level inverters and operation at higher dc voltages using series connected semiconductor switches. Owing to the various advantages of space vector pulse width modulation and multilevel inverters a series of global research activities have been spurred, especially in Europe and U.S., resulting several publications, patents, and applications. However, despite almost 20 years of research into the multilevel inverters some critical issues like harmonic elimination and capacitor voltage balancing need further study[4].

The series SVPWM method has been reported to easily implement SVPWM for the MLCI. In an SVPWM is proposed for hybrid inverters consisting of neutral point clamp and H-bridge inverters to improve output voltage quality and efficiency. As with two-level inverters, it is also possible to implement carrier-based SVPWMs which are equivalent to traditional SVPWMs by injecting a common offset voltage to the three-phase references. In some methods to calculate the offset voltages to achieve the optimal space vectors switching sequence are addressed. The performances of a carrier-based PWM and an SVPWM are compared, and a PWM scheme is proposed to obtain optimal output voltage in the multilevel inverter in[2].

In this paper presents the novel single carrier based SVWM strategy applied to five level, seven level, nine level and eleven level inverters are compared for THD. The paper mainly deals with the computation and the comparison of the motor harmonic losses of single carrier based conventional SVPWM solutions and with the selection of the solutions providing the best results. Finally, the drive harmonic losses, stator current, torque ripples, speed of the induction motor will be compared for all level inverters.

2 Generalized a novel single carrier based SVPWM techniques for cascaded multilevel inverter

Fig. 1: Illustrates the single carrier multi level modulation strategy. The modulation signals have the same frequency \( f_o \) and amplitude \( A_m \). The sinusoidal signals are sampled by a triangular carrier signal with frequency \( f_c \) and amplitude \( A_c \) once every cycle. Intersection between the sampled modulation signals and the carrier signal defines the switching instant of the PWM pulses. In order to ensure quarter wave symmetric properties of the PWM output waveform, the starting point of the modulation signals is phase shifted by one period of the carrier wave, in addition the frequency modulation ratio \( m_f \) must also be even number[8].

The single carrier PWM method offers a good opportunity for the realization of the Three-phase inverter control. In case of the five-level, seven-level, nine-level and eleven-level inverters it is better to use the single carrier PWM method with three carrier waves. In such case the motor harmonic losses will be considerably lower. The single carrier SPWM voltage switching scheme is selected in this paper because this method offers the advantages of effectively doubling the switching frequency of the inverter voltage. A particular advantage of the single carrier PWM approach is that, this method reduces the harmonics in the three phase inverter[12]. That means, selecting single carrier PWM as switching scheme in the proposed inverter is appropriate as there is no filter at the inverter output compared to other SPWM techniques. In this scheme, the triangular carrier waveform is compared with two reference signals which are positive and negative signal. The basic idea to produce SPWM with single carrier voltage switching is shown in Fig. 3: The different between the Bipolar SPWM generators is that the generator uses another comparator to compare between the inverse reference waveform \(-V_r\). For an N-level inverter, \( m_a \) and \( m_f \) for the single carrier multilevel modulation strategy are defined as the modulation index is the ratio of peak magnitudes of the modulating signal \( V_m \) and the carrier signal:

\[
m_a = \frac{V_m}{V_c}.
\]

The modulation index in SPWM technique for cascaded multilevel inverter configuration is given by:

\[
m = \frac{V_m}{(N-1)V_c}.
\]
Where $N$ is number of levels. For under modulation $0 < m < 1$. Generally, over modulation is not desired because of the presence of the lower frequency harmonics in the output voltage and subsequent distortion in the load current. It is the ratio of frequency of the triangular carrier signal $f_c$ to the frequency of sinusoidal reference signal $f_s$. It controls harmonics in the output voltage.

$$mf = \frac{f_c}{f_s}.$$ (3)

In the SPWM scheme for two-level inverters, each reference phase voltage is compared with the triangular carrier and the individual pole voltages are generated, independent of each other\cite{10, 14}. To obtain the maximum possible peak amplitude of the fundamental phase voltage, in linear modulation, a common mode voltage, $T_{offset}$, is added to the reference phase voltages shown in Fig. 2: Where the magnitude of $T_{offset}$ is given by

$$V_{offset} = \frac{-(V_{max} + V_{min})}{2}$$ (4)

$V_{max}$ is maximum of $V_{AN}, V_{BN}, V_{CN}$

$V_{min}$ is minimum of $V_{AN}, V_{BN}, V_{CN}$.

In equation, $V_{max}$ is the maximum magnitude of the three sampled reference phase voltages, while $V_{min}$ is the minimum magnitude of the three sampled reference phase voltages, in a sampling interval. The addition of the common mode voltage, $V_{offset}$, results in the active inverter switching vectors being centered in a sampling interval, making the SPWM technique equivalent to the modified reference PWM technique\cite{3}. Above Equation is based on the fact that, in a sampling interval, the reference phase which has lowest magnitude (termed the min-phase) crosses the triangular carrier first, and causes the first transition in the inverter switching state. While the reference phase, which has the maximum magnitude (termed the max-phase), crosses the carrier last and causes the last switching transition in the inverter switching states in a two level modified reference PWM scheme\cite{7}.

Thus the switching periods of the active vectors can be determined from the (max-phase and min-phase) sampled reference phase voltage amplitudes in a two-level inverter scheme\cite{15}. The SPWM technique, for multilevel inverters, involves comparing the reference phase voltage signals with a number of symmetrical level-shifted carrier waves for PWM generation. It has been shown that for an n-level inverter, n-1 level shifted carrier waves are required for comparison with the sinusoidal references\cite{6}. To obtain the maximum possible peak amplitude of the fundamental phase voltage in linear modulation, the procedure for this is given in\cite{1}, an offset time, offset $T$, is added to the reference phase voltages where the magnitude of $V_{offset}$ given by:
Fig. 2: The reference signals are added with an offset \( V_{offset1} \)

\[
T_a = \frac{- (V_a * T_s)}{V_{dc}}, \tag{5}
\]
\[
T_b = \frac{- (V_b * T_s)}{V_{dc}}, \tag{6}
\]
\[
T_c = \frac{- (V_c * T_s)}{V_{dc}}. \tag{7}
\]

\( T_a, T_b \) and \( T_c \) are the imaginary switching time periods proportional to the instantaneous values of the reference phase voltages.

\[
T_{offset} = \left[ \frac{T_o}{2} - T_{min} \right], \tag{8}
\]
\[
T_o = [T_s - T_{offset}], \tag{9}
\]
\[
T_{offset} = [T_{max} - T_{min}]_. \tag{10}
\]

Fig. 3: The comparison of modulated wave with carrier wave in case of conventional SVPWM

The generation of modulating and triangular wave of the novel single carrier based SVPWM technique shown in Fig. 4: We can observe the Output currents at the load using single carrier PWM technique show in Fig. 6 and also switching pulses generation using single carrier based PWM techniques shown in Fig. 5.

2.1 Proposed n-level cascaded h-bridge multilevel inverter

The three phase N-level cascaded multilevel inverter (CMI) or Series H-bridge Multi-Level Inverter topology shown in Fig. 7: Each cell contains four active switching device and a minimum of one dc capacitor to
form a single-phase H-bridge inverter. The different cells are connected as depicted in Fig. 7: To construct a three-phase configuration.

With this configuration, each cell in a leg will provide three-level output phase voltage \( V_{aN} \), \( V_{bN} \) and \( V_{cN} \) and five level line voltages \( V_{ab}, V_{bc} \) and \( V_{ca} \). The number of incremental voltage step is increased by connecting additional cell in series, where the number of phase voltage is formulated as \((n^{th} \text{ cell } \times 2)+1\), and the number of levels in line voltage are \(2M - 1\), where \(M\) is the number of level in phase voltage. This type of multilevel inverter topologies can reduce the number of switching devices, but it requires multiple isolated dc supply to operate the converter \cite{9}. The output voltage of the inverter shown in equation (11):

\[
V_{01} = V_{d1} + V_{d2} + \ldots + V_{dn}.
\] (11)
2.2 Simulation results and discussions for single carrier PWM techniques

The validity of the proposed synthesis approach is verified by the simulation using MATLAB/simulation. The output-voltage waveform has a five level, seven level, nine level and eleven level output voltage waveform by the combination of the series connected H-bridge in sequence. The simulation diagram of N-level multilevel inverter is shown in Fig. 7. The gate signals applied to the switches of proposed inverter are shown in Fig. 3. The output voltage waveform with induction motor load is very similar to a sinusoidal one, owing to a large number of output voltage levels. The cascaded H bridge MLI implementing proposed single carrier SPWM techniques fed induction motor.

Fig. 8: Indicates output stator current of the load, we can observe the system is unstable from 0 to 0.1 sec. Due to transient behavior of the system at the starting from 0.15 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to five level inverter has shown in Fig.
9. From the figure it can be seen that the steady state operation of system has achieved at 0.17 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for single carrier SPWM techniques. The simulated five level cascaded H-bridge MLI fed to induction motor load. Each phase consist of two H-bridges to generated 5 levels in phase voltages and 9 levels in line voltages and we can observe the total harmonic distortion of the line voltages like that 23.13%. shown in Fig. 10:

![Fig. 10: Total Harmonic Distortion (THD)](image)

Fig. 11: Stator current for seven level inverter

Fig. 12: Speed and torque for seven level inverter

Fig. 13: THD for seven level inverter

Fig. 11 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.25 sec. Due to transient behavior of the system at the starting from 0.27 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to seven-level inverter has shown in Fig. 12. From the figure it can be seen that the steady state operation of system has achieved at 0.28 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for single carrier SPWM techniques. the simulated seven level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 11 and Fig. 12. Each phase consist of three H-bridges to generated seven levels in phase voltages and 13 levels in line voltages and we can observe the total harmonic distroction of the line voltages like that 15.33% shown in Fig. 13:

Fig. 14 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.45 sec. Due to transient behavior of the system at the starting from 0.48 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to nine-level inverter has shown in Fig. 15. From the figure it can be seen that the steady state operation of system has achieved at 0.36 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for single carrier SPWM techniques. the simulated nine level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 14: and Fig. 15: Each phase
consist of four H-bridges to generate nine levels in phase voltages and 17 levels in line voltages and we can observe the total harmonic distortion of the line voltages like that 12.81% shown in Fig. 16:

Fig. 17: Indicates output stator current of the load, we can observe the system is unstable from 0 to 0.37 sec. Due to transient behavior of the system at the starting from 0.36 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to eleven-level inverter has shown in Fig. 18: From the figure it can be seen that the steady state operation of system has achieved at 0.38 sec. A three phase induction motor considered as load for scheme. the separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for single carrier SPWM techniques. the simulated eleven level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 17: and Fig. 18. Each phase consist of five H-bridges to generate eleven levels in phase voltages and 21 levels in line voltages and we can observe the total harmonic distortion of the line voltages like that 10.62% shown in Fig. 19:
2.3 Simulation results and discussions for a novel single carrier based SVPWM techniques

The simulation diagram of N level multilevel inverter is shown in Fig. 7. The gate signals applied to the switches of proposed inverter are shown in Fig. 3. The output voltage waveform with induction motor load is very similar to a sinusoidal one, owing to a large number of output voltage levels. The cascaded H bridge MLI implementing proposed novel single carrier based SVPWM techniques fed induction motor.

Fig. 19: THD for eleven level inverter

Fig. 20: Stator current for eleven level inverter

Fig. 21: Speed and torque for eleven level inverter

Fig. 22: THD for eleven level inverter

Fig. 20 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.1 sec. Due to transient behavior of the system at the starting from 0.15 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to five-level inverter has shown in Fig. 21. From the figure it can be seen that the steady state operation of system has achieved at 0.15 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for
each H-bridge and the switching frequency is 1kHz considered for modified single carrier SPWM techniques. the simulated five level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 20 and Fig. 21. Each phase consist of two H-bridges to generated five levels in phase voltages and 9 levels in line voltages and we can observe the total harmonic distroction of the line voltages like that 18.93%.shown in Fig. 22.

![Fig. 23: Stator current for eleven level inverter](image)

![Fig. 24: Speed and torque for eleven level inverter](image)

![Fig. 25: THD for eleven level inverter](image)

Fig. 23: Indicates output stator current of the load, we can observe the system is unstable from 0 to 0.2 sec. Due to transient behavior of the system at the starting from 0.2 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to seven level inverter has shown in Fig. 24. From the figure it can be seen that the steady state operation of system has achieved at 0.27 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for modified single carrier SPWM techniques. the simulated seven level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 23 and Fig. 24. Each phase consist of three H-bridges to generated seven levels in phase voltages and 13 levels in line voltages and we can observe the total harmonic distroction of the line voltages like that 13.28%.shown in Fig. 25.

Fig. 26 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.42 sec. Due to transient behavior of the system at the starting from 0.42 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to nine level inverter has shown in Fig. 27. From the figure it can be seen that the steady state operation of system has achieved at 0.38 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for modified single carrier SPWM techniques. the simulated nine level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 26 and Fig. 27. Each phase consist of four H-bridges to generated nine levels in phase voltages and 17 levels in line voltages and we can observe the total harmonic distroction of the line voltages like that 10.77%.shown in Fig. 28:

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Fig. 26: Stator current for eleven level inverter

Fig. 27: Speed and torque for eleven level inverter

Fig. 28: THD for eleven level inverter

Fig. 29: Stator current for eleven level inverter

Fig. 30: Speed and torque for eleven level inverter

Fig. 31: THD for eleven level inverter

Fig. 29 indicates output stator current of the load, we can observe the system is unstable from 0 to 0.36 sec. Due to transient behavior of the system at the starting from 0.36 sec. System has attained steady state conditions. The speed and torque characteristics of induction motor fed to eleven-level inverter has shown in Fig. 30. From the figure it can be seen that the steady state operation of system has achieved at 0.36 sec. A three phase induction motor considered as load for scheme. The separate DC voltage sources are set to 100V for each H-bridge and the switching frequency is 1kHz considered for modified single carrier SPWM techniques. the

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simulated eleven level cascaded H-bridge MLI fed to induction motor load and observe the variation of stator currents, torque, reference speed and actual speed of the induction motor shown in Fig. 29 and Fig. 30; Each phase consist of five H-bridges to generated nine levels in phase voltages and 21 levels in line voltages and we can observe the total harmonic distortion of the line voltages like that 10.13%. shown in Fig. 31.

The simulation of output voltage total harmonic distortion for the case of \( M_f = 200 \), \( M_a = 0.5 \) are illustrated. The comparison the harmonic profile of the proposed modulation technique with the modified single carrier scheme. it can be observed that the proposed technique produces an identical total harmonic distortion to the modified single carrier scheme for major harmonics. It can be suggested that both strategies produce harmonic components of the same magnitudes and frequency despite the obvious different between the two modulation principles. The total harmonic distortion waveforms obtained from the simulation results using MATLAB/SIMULINK and compared the all levels (five, seven, nine and eleven) of the cascaded multi level inverter. The comparison are made for the total harmonic distortion wave forms based on variations of parameters amplitude modulation (\( m_a \)) and frequency modulation (\( m_f \)), and we can observe the three phase stator currents, torque and speed of the induction motor for all levels of the inverter. The Comparison of THD analysis for both modulation techniques (single carrier and modified single carrier) of a three-phase cascaded inverter fed to induction motor shown in Table 2.

Table 1: Comparison of total harmonic distortion of the difference single carrier PWM techniques

<table>
<thead>
<tr>
<th>S.NO</th>
<th>Output voltage levels</th>
<th>Single carrier PWM (%THD)</th>
<th>Single carrier based conventional SVPWM (%THD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Five level</td>
<td>23.17</td>
<td>18.93</td>
</tr>
<tr>
<td>2</td>
<td>Seven level</td>
<td>15.33</td>
<td>13.28</td>
</tr>
<tr>
<td>3</td>
<td>Nine level</td>
<td>12.81</td>
<td>10.77</td>
</tr>
<tr>
<td>4</td>
<td>Eleven level</td>
<td>10.62</td>
<td>10.13</td>
</tr>
</tbody>
</table>

3 Conclusion

In this paper the novel single carrier pulse width modulation strategy has presented for modular cascaded H-bridge multilevel inverter topology. The reference signals for PWM are generated by using modified single carrier PWM techniques. This method does not involve region identifications, sector identifications for switching vector determination as like in conventional SVPWM technique. It also shown improved fundamental output by using this technique can be seen in FFT analysis. The comparison of general single carrier SPWM and modified single carrier SPWM are applied to three phase Cascaded inverter of various levels are presented. The waveforms clearly depicting that almost all the control strategies are functioning well in controlling the stator currents, speed, torque and total harmonic distortion but the novel single carrier is most effective in terms of torque ripple minimization and effective DC-link utilization.

Table 2: System parameters of the induction motor

<table>
<thead>
<tr>
<th>S.NO</th>
<th>Parameters</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Input voltage</td>
<td>400V RMS</td>
</tr>
<tr>
<td>2</td>
<td>Inverter voltage</td>
<td>100V</td>
</tr>
<tr>
<td>3</td>
<td>Rotor speed</td>
<td>1440RPM</td>
</tr>
<tr>
<td>4</td>
<td>Fundamental frequency</td>
<td>50Hz</td>
</tr>
<tr>
<td>5</td>
<td>Switching frequency</td>
<td>1KHz</td>
</tr>
<tr>
<td>6</td>
<td>Amplitude modulation</td>
<td>0.5</td>
</tr>
<tr>
<td>7</td>
<td>Frequency modulation</td>
<td>200</td>
</tr>
</tbody>
</table>
References


