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Modelling and simulation of high step up interleaved DC-DC converter for stand-alone PV system

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Abstract. In this paper, an interleaved high step up DC-DC converter is presented for a 3ϕ stand-alone PV system. The converter consists of an interleaved stage, a voltage lift capacitor and a voltage multiplier cell (VMC) which is integrated with the secondary winding of coupled inductor. By using a coupled inductor with a turns ratio of 2.5 and operating the switches at 0.55 duty cycle, a voltage gain of 17 is obtained. The operating principle, characteristic waveforms, steady state analysis, design details and simulation results of a 60V/1100V, 3kW and 100kHz converter are elaborated.

Keywords: high gain, interleaved boost converter, voltage multiplier cell, stand-alone PV systems

1 Introduction

To electrify the rural and remote areas, stand-alone PV systems play an important role. In general, PV panels for a stand-alone system are placed on the roof tops of houses / buildings. The output from the PV panel may be decreased due to partial shading when they are connected in series. To overcome this drawback, PV panels are connected in parallel configuration. However, the maximum output voltage of the system is of the order of 60V[1, 7, 14–16]. Considering the safety of the personnel, parallel connected configurations are preferred for a stand-alone PV system. Applications which are fed from parallel connected PV sources require high voltage step up DC-DC converters with higher power handling capability to meet the load requirements.

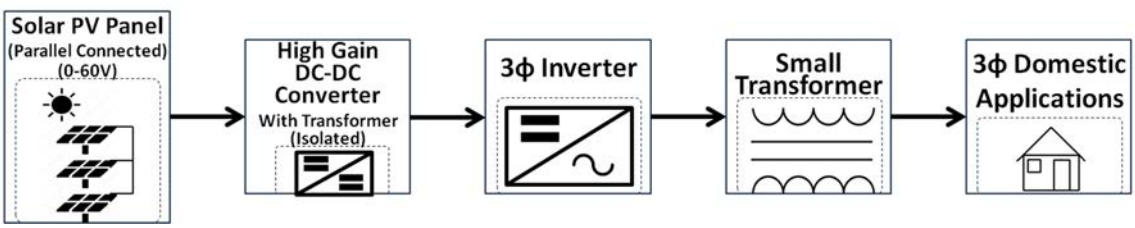

Fig. 1: Stand-alone PV system with isolated DC-DC converter

Conventionally, the low voltage DC output from PV panels is converted into AC using an inverter. A transformer is used to fulfill the voltage gain requirements before connecting to loads. To reduce the size of the system, the transformer can be eliminated by introducing a high gain DC-DC converter as shown in Fig. 1. Classical boost converters are not capable of offering voltage gain higher than 4 because of various limitations[12]. Hence, hybrid combinations of various boost techniques are used to acquire high gain.

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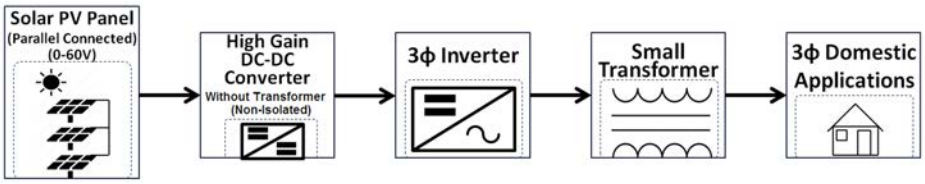

Fig. 2: Stand-alone PV system with non isolated DC-DC converter

Some popular techniques to enhance the voltage gain are (i) VMCs, (ii) diode-capacitor cells and (iii) switched capacitors. The number of diodes and capacitor requirement increases in VMC and diode capacitor cell based topologies along with higher voltage gain requirement[4, 8–10, 13, 19]. Consequently, total voltage drop on the devices increases leading to poor voltage regulation. Multi-coupled converters offer a gain of about 10 with power handling capability limited to 1kW[3, 5].

Switched capacitor based converters offer higher gain with better regulation and compact size due to the elimination of inductors. However, voltage balancing on the output capacitors is troublesome[17]. Converters employing other techniques like built in transformer[18], dual coupled inductors[18], and WCCI[11] increase the design and control complexity. Few converters which operate at higher power levels provide only very low voltage gain[2, 6]. In this paper, a hybrid high gain high power DC-DC converter to suit the needs of PV fed stand-alone system is presented. The circuit details and operating principle of the proposed converter are presented in Section 2 and Section 3 respectively. Section 4 provides the design details while Section 5 is used to present the simulation results and their inferences. Finally, the concluding remarks are presented in Section 6.

2 Proposed converter

The proposed converter shown in Fig. 3(a) is derived by combining high step up interleaved converter, coupled inductors and voltage multiplier cell. The primary windings of the coupled inductors form the input inductors of the interleaved boost converter. In order to achieve high voltage gain, the secondary windings of the coupled inductors are connected in series. Further, the secondary windings of coupled inductors are entrenched with the two multiplier cells formed by capacitors C_{M1}, C_{M2}, and diodes D_{M1} and D_{M2}.

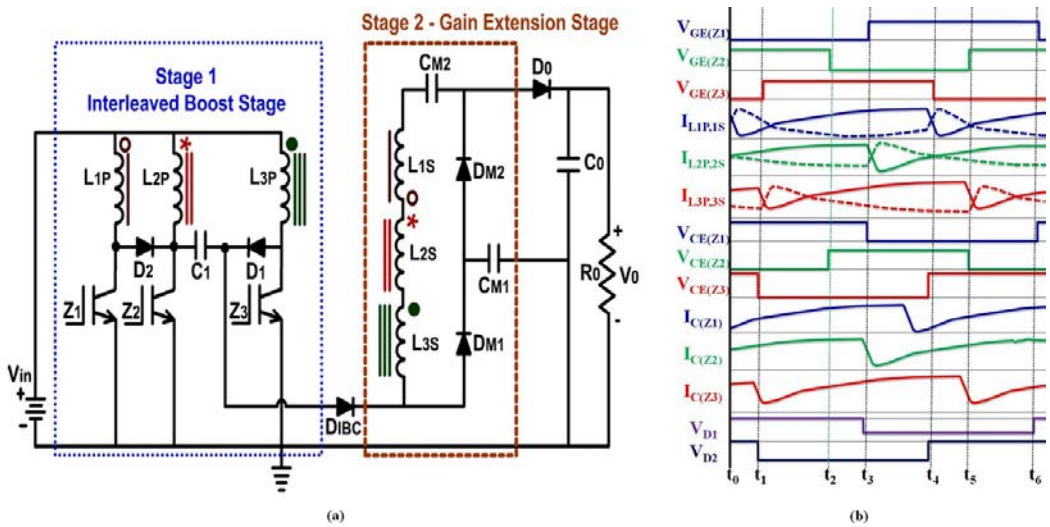

Fig. 3: (a) Proposed converter circuit (b) Characteristic Waveforms

3 Operating principle

The analysis and operating principle of the proposed converter is discussed in detail in this section with the following assumptions.
Assumptions:

(1) The proposed converter is constructed using ideal switches and diodes.
(2) The proposed converter operates in continuous conduction mode.

To understand the working of the proposed converter, a single switching cycle is divided into six time intervals. The operation of proposed converter in each interval is discussed in the following modes. The equivalent circuit of the proposed converter in various modes is shown in Fig. 3.

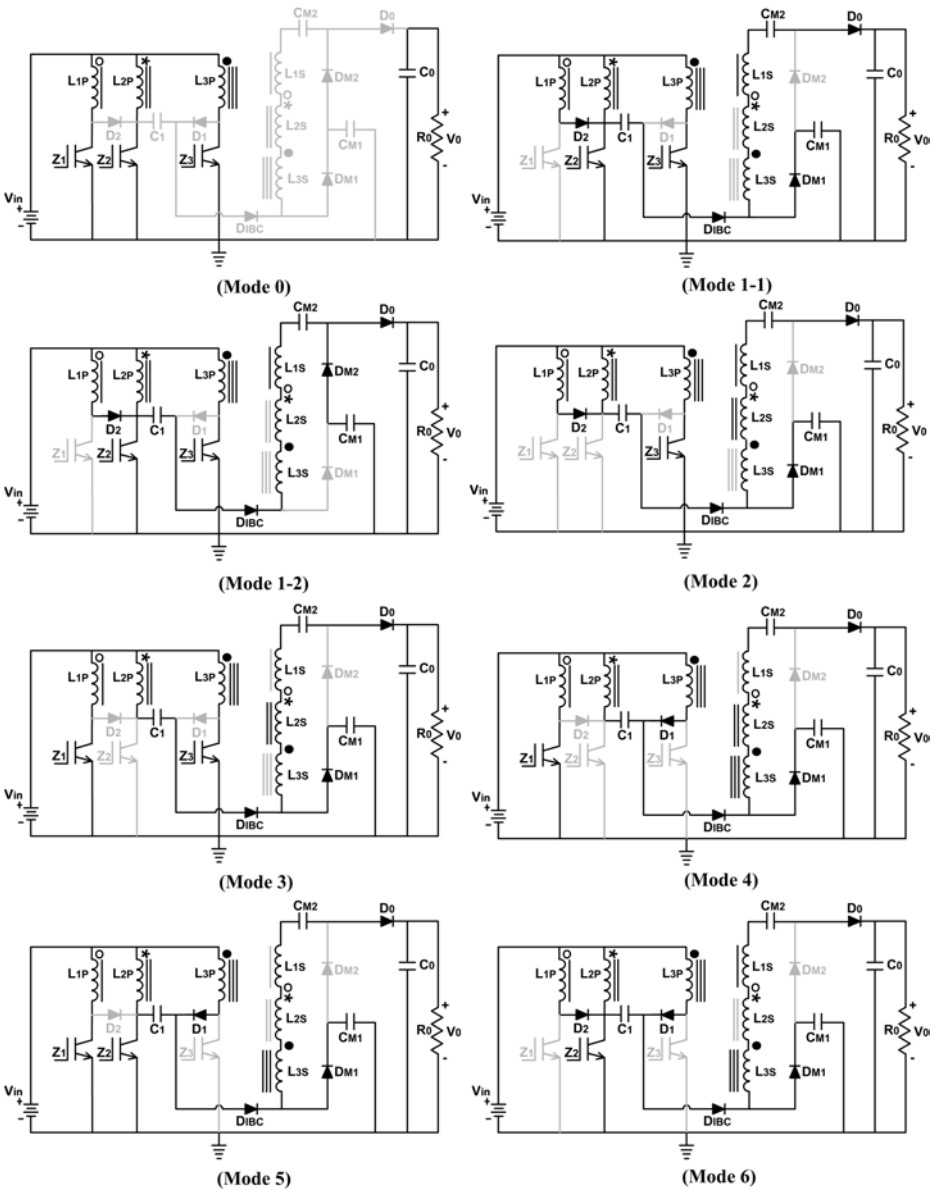

Fig. 4: Modes of operation of the proposed converter

Mode 0:

Before t_0, all the power switches Z_1, Z_2 and Z_3 are turned ON in order to charge the primary windings L_{1P}, L_{2P} and L_{3P} of coupled inductors to a voltage equal to V_{in}. All the diodes remain OFF. Since the primary

windings of all the coupled inductors are in charging state, no energy is transferred to the secondary winding during this mode. The output capacitor C_0 feeds the load R_0. Since switch is Z_1 is ON, the voltage across the primary winding L_{1P} the of coupled inductor is given by

$$V_{L_{1P}} = V_{in}. \tag{1}$$

The voltage across the diodes D_1, D_{M1} and D_0 is given by

$$v_{D_1} = V_{C_1}, \tag{2}$$
$$v_{D_{M1}} = V_{C_{M1}} - V_{C_1}, \tag{3}$$
$$v_{D_0} = V_0 - V_{C_{M1}}. \tag{4}$$

Mode 1-1 :

Switch Z_1 remains in OFF state and other two switches Z_2 and Z_3 remain ON. Stored energy in the primary winding L_{1P} is begins to get transferred to its secondary winding L_{1S}. Energy transfer from L_{1P} to L_{1S} is through D_2, C_1 and DIBC. Further, the VMC network which forms the second stage of the proposed converter transfers its stored energy to the load through C_{M2} and D0, thus offering voltage gain extension.

In this mode, the working of IBC which forms the first stage of the proposed converter is similar to a conventional boost converter. Therefore, the voltage across the lift capacitor C_1 is given by

$$V_{C_1} = \frac{1}{1-D} V_{in}. \tag{5}$$

Mode 1-2 :

The diode D_{M1} is forward biased till the capacitor C_{M1} is completely charged. Once voltage across capacitor C_{M1} reaches its maximum value, diode D_{M1} is reverse biased and diode D_{M2} becomes forward biased and turns ON. Stored energy in C_{M1} is discharged to the load through diode D_{M2} and D_0. Current through capacitor C_{M2} is given by

$$i_{C_{M2}}(t) = \frac{(nV_{L_{1P}} - V_{C_{M2}})}{n^2 (L_{1P} + L_{2P} + L_{3P})} \times t. \tag{6}$$

Current through diode D_2 is same as the current through primary winding L_{1P} and D_{M1}. Inductor L_{1P} is linearly discharging and inductor L_{2P} is charging linearly at the same rate. Hence, the current through D_2 decreases linearly at the same rate in which current through D_{M1} increases. Therefore, current flowing through diode D_1 can be written as

$$i_{D_1}(t) = n \left(i_{DM1}(t) + i_{CM2}(t) \right). \tag{7}$$

Inductors L_{2P} and L_{3P} are in charging state as switches Z_2 and Z_3 are conducting.

Mode 2:

In this mode, switches Z_1 is maintained in OFF state. Z_2 is turned ON and switch Z_3 continues to remain in ON state. The diode D_2 remains in ON state till switch Z_1 is turned ON. Stored energy in primary winding L_{1P} and L_{2P} of the coupled inductors is transferred to the load through the voltage lift capacitor C_1 and the gain extension stage. The voltage lift capacitor C_1 is charged to $[2/(1-D)] \times V_{in}$ through D_2. Switch Z_3 is conducting and diode D_1 remains in reverse biased condition similar to the earlier mode. Current through switch Z_3 can be derived as

$$i_{Z_3} = i_{L_{3P}}(t) = \left[\frac{n\left(V_{L_{1P}} + V_{L_{2P}}\right) - V_{C_{M2}}}{n^2\left(L_{1P} + L_{2P} + L_{3P}\right)}\right] \times t. \tag{8}$$

Mode 3 :

Switches Z_1 and Z_3 are ON while switch Z_2 is turned OFF. Diodes D_1 and D_2 are reverse biased. Inductor L_{2P} discharges to charge secondary winding of coupled inductor L_{2S} and multiplier capacitor C_{M1} through diode D_{M1}. Once the capacitor C_{M1} is completely charged, diode D_{M2} will be forward biased. Stored energy in C_{M1} will be transferred to C_{M2} and C_0 similar to Mode 1-2. Current through capacitor C_{M2} is governed by

$$i_{C_{M2}}(t) = \left[\frac{V_0 - V_{C_1} - NV_{L_{1P}} - V_{C_{M2}}}{n^2\left(L_{1P} + L_{2P} + L_{3P}\right)}\right] \times t. \tag{9}$$

Mode 4:

Switch Z_1 is continues to remain in ON state. Switches Z_2 and Z_3 are turned OFF. Primary winding L_{1P} of the coupled inductor continues to charge through switch Z_1 till the voltage across it becomes equal to the input voltage V_{in}. Current through switch Z_1 is expressed as

$$i_{Z_1}(t) = ni_{D0}(t) = \left[\frac{V_0 - V_{C_1} - nV_{L_{1P}} - V_{C_{M2}}}{n^2\left(L_{1P} + L_{2P} + L_{3P}\right)}\right] \times t. \tag{10}$$

Mode 5:

Switch Z_1 continues to remain in ON state while switch Z_2 is turned ON. As switch Z_3 remains in OFF state, diode D_2 becomes forward biased and stored energy in primary winding L_{3P} of coupled inductor starts discharging linearly to the secondary winding L_{3S} of the coupled inductor. The current through diode D_2 is expressed as

$$i_{D_2}(t) = -ni_{D_0}(t). \tag{11}$$

The operation of the VMC in the proposed converter is similar to the earlier modes.

Mode 6:

Switch Z_1 is turned OFF. Z_3 continues to remain in OFF state while Z_2 still continues to conduct and enables L_{2P} to charge towards the input voltage V_{in}. Diodes D_1 and D_2 are conducting. Primary windings L_{1P} and L_{3P} of coupled inductors discharge to the load while maintaining the voltage across the lift capacitor as and L_{1P} $[3/(1-D)]V_{in}$. The secondary windings of coupled inductor and capacitor C_{M2} extend the voltage gain as mentioned earlier. Current through D_0 is controlled by primary windings of coupled inductors and is expressed as

$$i_{D_0}(t) = \left[\frac{3V_{in} + V_{C_{M2}} - DV_{C_{M2}} - V_0 + DV_0}{n^2\left(1-D\right)\left(L_{1P} + L_{2P} + L_{3P}\right)}\right] \times t. \tag{12}$$

The commencement of new switching cycle is marked by the end of Mode 6.

4 Steady-state analysis and design details

4.1 Voltage gain

Both stages of the proposed converter contribute in delivering high step up voltage at the load.

$$M = M_{\text{Stage1}} + M_{\text{Stage2}}. \tag{13}$$

Voltage gain offered by IBC is given by

$$M_{\text{Stage1}} = \left[\frac{3}{1-D}\right]. \tag{14}$$

Voltage gain offered by gain extension stage is derived as

$$M_{\text{Stage2}} = (V_{L1S} + V_{CM2}) \times \left(\frac{1}{1-D}\right) = \frac{2n}{1-D}. \tag{15}$$

Therefore, the total voltage gain can be expressed as

$$M = \left(\frac{V_{out}}{V_{in}}\right) = \frac{3+2n}{1-D}. \tag{16}$$

4.2 Selection of turns ratio and duty ratio

In a stand-alone PV system supplying domestic loads, output voltage of 3ϕ inverter should be 415V AC as per the standards. In a 3ϕ VSI operating in 180° conduction mode, RMS n^{th} component of line voltage is given by

$$V_{Ln} = \frac{4V_{dc}}{\sqrt{2}n\pi} \sin\frac{n\pi}{3}. \tag{17}$$

In order to get the standard AC output voltage from the 3ϕ inverter, the magnitude of DC input voltage fed to the 3ϕ VSI from the DC-DC converter should be in the range of 978 V to 734V if modulation index 'm' of the inverter varies between 0.6 to 0.8.

Therefore, the turns ratio 'n' of the coupled inductors and duty ratio 'D' of the proposed high gain high power DC-DC converter is selected from the plot shown in Fig. 5(a) to meet the standard voltage level at the AC side. Turns ratio 'n' of the proposed converter is expressed as

$$n = \frac{M - MD - 3}{2}. \tag{18}$$

The output voltage of the proposed converter for various percentage of load is shown in Fig. 5(b). When the load is increased from rated load (3kW) to 125% of rated load, voltage regulation of 6% is achieved. This clearly demonstrates the power delivering capability of the proposed converter.

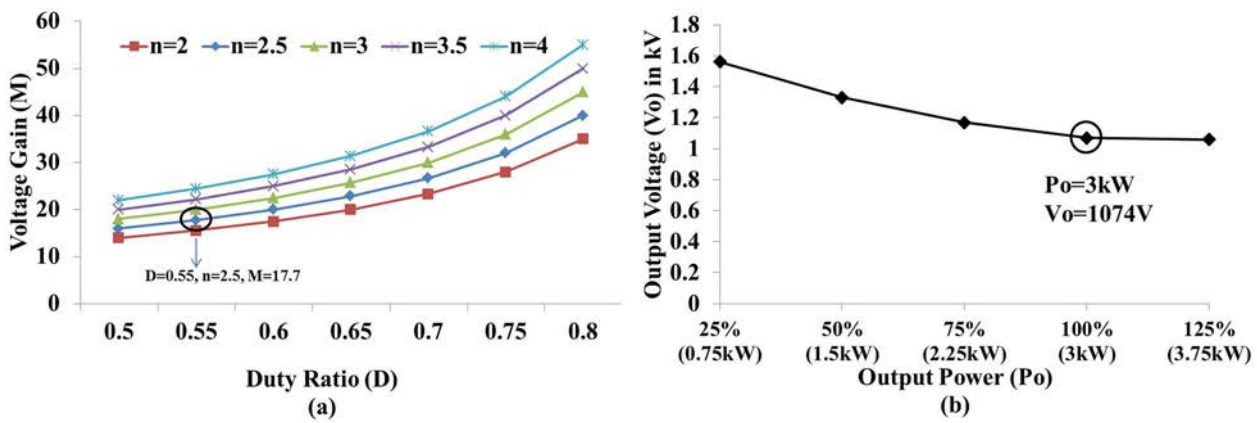

Fig. 5: (a): Voltage gain (M) Vs Duty cycle (D) (b): Output Voltage (V0) Vs Output Power (P0)

4.3 Voltage and current stress

Due to the employment of voltage lift technique, the switches experience different voltage stress levels. Voltage stress on the power switches Z_1 and Z_2 is equal to voltage across the lift capacitor C_1. Therefore, the voltage stress is expressed as

$$V_{Z_1} = V_{Z_2} = \frac{V_0}{\left(1 + \frac{2}{3}n\right)}. \tag{19}$$

Voltage across switch Z_3 is given by

$$V_{Z_3} = \frac{V_0}{(3 + 2n)}. \tag{20}$$

Voltage stress on the output diode D_0 is given by

$$V_{D_0} = V_{D_{M2}} = V_O - V_{C_{M1}}. \tag{21}$$

From Mode 4, the current through switch Z_1 can be expressed as

$$i_{Z_1}(t) = n i_{D_0}(t) = \left[\frac{V_0 - V_{C_1} - NV_{L_{1P}} - V_{C_{M2}}}{n^2\left(L_{1P} + L_{2P} + L_{3P}\right)}\right] \times t. \tag{22}$$

The current through switches Z_2 and Z_3 will be half of current through switch Z_1.

4.4 Design of passive components

The design of multiplier capacitors (C_{M1}, C_{M2}) and the clamp capacitor (C_c) depends on their voltage ripple requirement. Considering the output power (P_0), output voltage (V_0), operating frequency (f_s) and output voltage ripple (ΔV_C), the capacitor value is given by

$$C = \frac{P_o}{V_o \Delta V_C f_s}. \tag{23}$$

The rating of coupled inductor is determined from the rate of fall of diode reverse recovery current. The output diode D_0 has to withstand the output voltage. Hence, the rate of fall of reverse recovery current is given by

$$\frac{diD_o}{dt} = \frac{V_o}{ML_{1P}}. \tag{24}$$

The values of L_{2P} and L_{3P} are made equal to L_{1P}. Depending on the turns ration 'n', the values of L_{1S}, L_{2S} and L_{3S} are computed.

4.5 Simulation results

The proposed converter was simulated using PSpice software with the following specifications: input voltage = 60V, output voltage = 1066 V, output power = 3 kW, switching frequency $f_S = 100$ kHz. The duty ratio D was chosen as 0.55 and the corresponding turns ratio n was obtained as 2.5. The inductance values of coupled inductor at primary side (L_{1P}, L_{2P} and L_{3P}) were derived as 35 μH. Based on $n = 2.5$, the output inductances (L_{1S}, L_{2S} and L_{3S}) were computed as $218\mu H$. The multiplier and the clamping capacitors (C_{M1},

C_{M2} and C_c) were chosen to be 4.7 μF each. The load resistance was computed from the output voltage and power.

Fig. 6(a) shows the gate pulse pattern applied to power switches and the output voltage of the proposed converter. The output voltage ripple is very less and the proposed converter provides the desired voltage at the designed power level. Current through primary winding L_{1P} of coupled inductor shown in Fig. 6(b) is n times the current through its secondary winding and demonstrates their complimentary behavior. The currents through the primary windings (L_{2P}, L_{3P}), secondary windings (L_{2S}, L_{3S}) and the power switches Z_2 and Z_3 are shown in Figs. 7(a) and (b). Due to interleaving technique, the total current is shared by the switches. Further, the current flowing through the secondary winding is reduced due to the turns ratio (2.5) of the coupled inductor. Fig. 8(a) shows the voltage and current stress experienced by switch Z_3. Switches Z_1 and Z_2 experience similar stresses as given by Eq. (19).

To validate the design details of the power switches, voltage stress and current stress on switch Z_3 is shown in Fig. 8(a). The peak voltage stress across the switch adheres to expression (20). This is within safe limits and as expected. Since the switches are connected near the input side of coupled inductor and large power transfer is involved, the current through the switches is relatively large. However, due to practical availability of high current rated devices, no problems are envisaged during construction and testing of the experimental setup.

The voltage across the multiplier and the output capacitors are shown in Fig. 8(b). The voltage across multiplier capacitor C_{M1} is slightly less than the output voltage. This is in total agreement with the designed value obtained from Eq. (21).

Fig. 9 shows the efficiency curve of the proposed converter. At rated load, converter operates with a maximum efficiency of 88%. The major losses occur due to the leakage inductances and the multiplier diodes.

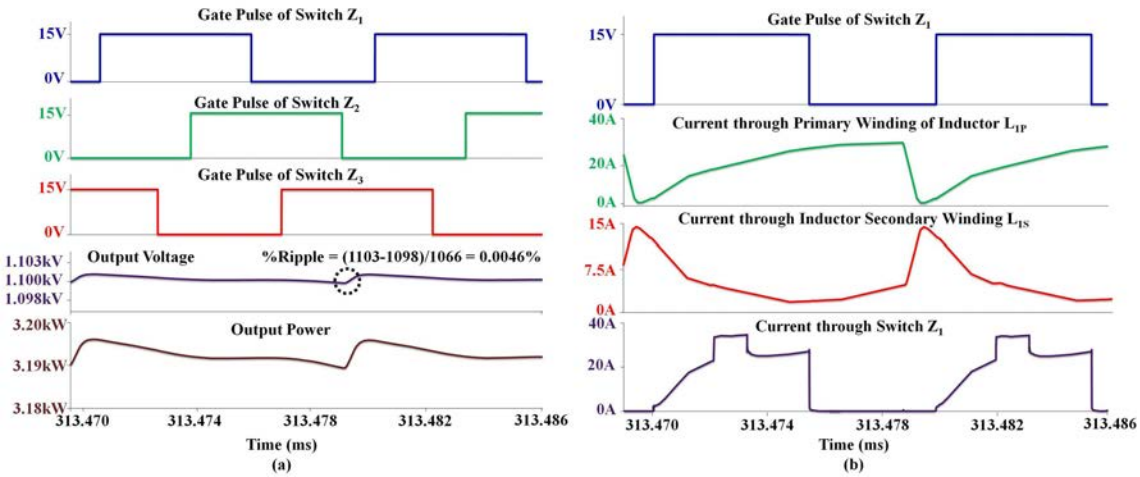

Fig. 6: (a): Gate pulses, output voltage and output power (b): Current through inductor L_2 and switch Z_2

5 Conclusion

The proposed converter offers a gain of 17 and is capable of operating at 3kW power. The converter is capable of operating from 60V input and provides 1.1kV at the output at 88% efficiency. The high gain and high power capability was achieved by the hybrid combination of 3 interleaved phases with coupled inductors, voltage lift capacitor and 1 VMC network. The proposed converter is modular in structure. The switches used in the converter are subjected to a maximum voltage stress which is only one-third of the output voltage. Due to interleaving technique, the total input current is shared among the interleaved phases. This results in a reduced current stress on the switches. Results obtained by simulating the proposed converter confirm the effectiveness of the adopted design procedure. The proposed converter proves to be an appropriate solution for a stand-alone PV system.

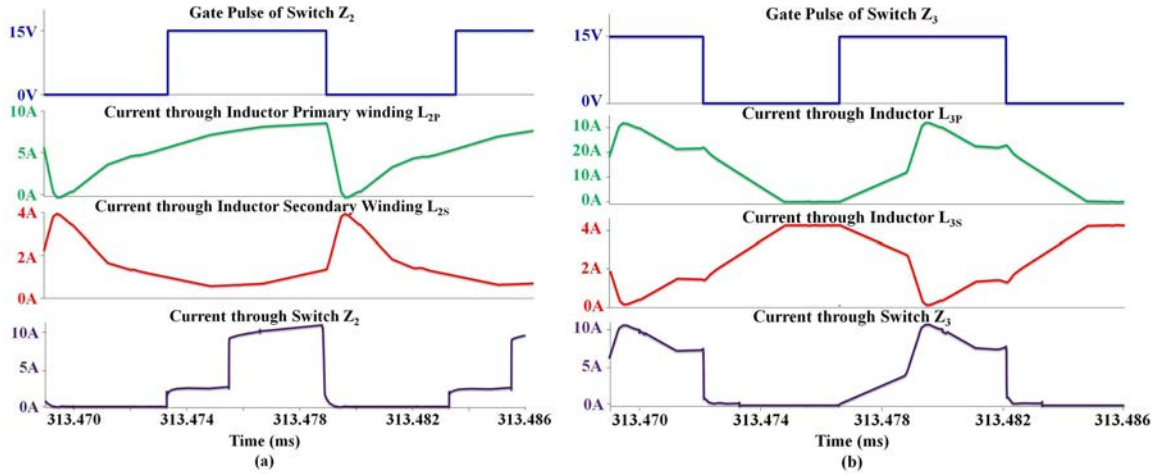

Fig. 7: .a: Current through Inductor L1 and Switch Z_1 (b): Current through Inductor L_3 and Switch Z_3

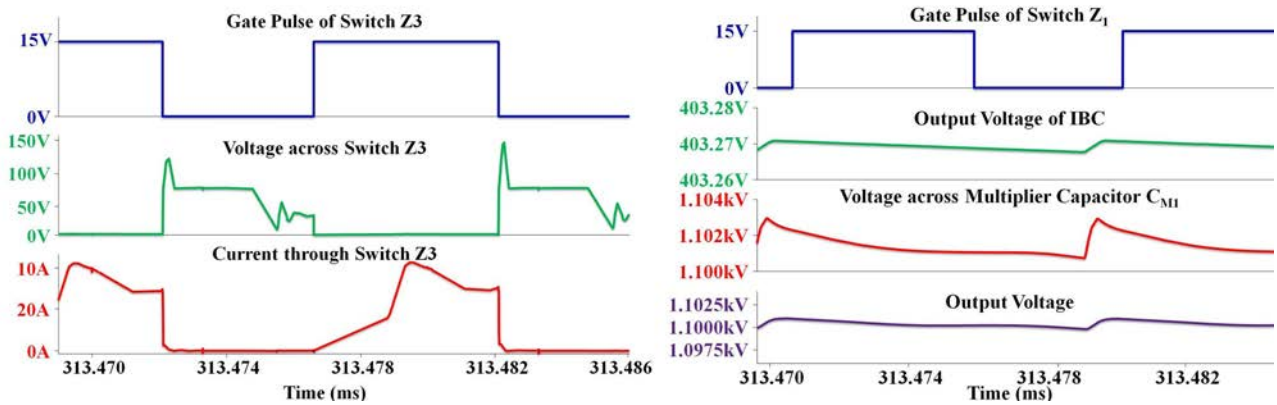

Fig. 8: (a): Voltage and Current Stress on Switch Z_3 (b): Voltage across Capacitors at Various Stages

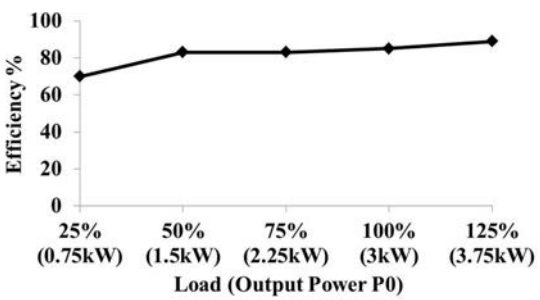

Fig. 9: Efficiency curve

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