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Modeling and control of split capacitor type elementary additional series positive output super lift Luo converter

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Abstract. DC/DC traditional converter voltage gain is limited with the duty ratio of the converter. High duty ratio will have narrow turnoff time, thereby considerable conduction and switching loss occurs. The High voltage gain requirement of the converter is needed to meet the demands of the renewable energy system with low input voltage. Super lift Luo converter is a new topology of DC/DC converter with its output voltage increasing in geometric progression. Super lift technique armed by split capacitors increases the output voltage in higher geometric progression. This paper focuses on the modeling and control of split capacitor type elementary additional series positive output super lift Luo converter. A state space averaging model of the proposed converter is carried out in order to provide a good line and load regulation. A PI controller is designed to control the duty ratio of switching pulse of the converter to stabilize the output for variation in line and load side. Simulation of the proposed converter is performed in MATLAB/SIMULINK. A prototype of the converter along with the controller is developed using analog PWM IC to validate the simulation results.

Keywords: split type elementary additional series positive output super lift converter (SEPOSLC), proportional-integral (PI) control, state space averaging

1 Introduction

High Step up DC-DC boost type converter will boost the low voltage input to a high voltage output. DC voltage level input from the sources such as fuel cell stacks, single PV module, battery sources and super capacitors are relatively low it should be boosted up to use in real time applications such as motor control, battery charging and uninterruptible power supplies. There are different topologies in dc-dc converters classified into isolated and non-isolated converter, in isolated converters high frequency transformer turns ratio is varied to boost the voltage ratio of the converter but limitation is system volume, leakage inductance and efficiency due to multistage DC-AC-DC conversion[9]. Non-isolated and non-coupled converters vary the voltage ratio by switching the energy storage elements with two topologies such as switched capacitor and switched inductor. Super lift Luo converter is a topology in which the voltage transfer gain is increased by cascading the energy storage elements in stages, Split type Elementary Additional Series Positive Output Super Lift Converter (SEPOSLC) is a modified topology of a positive output super lift Luo converter in which the output voltage increase in geometric progression from elementary to n series[7]. Advantages of super lift converter are reduced ripple voltage and current, high efficiency and voltage transfer gain. Output voltage in super lift converter is increased by pumping the energy stored in the inductors and capacitors by splitting the input side capacitor. Input capacitor is split into α parts, if $\alpha = 2$ the capacitor is split into two capacitors and charged to the supply voltage during ON condition of the switch[6].Positive output super lift Luo converter is divided into two series namely main series and additional series each series is subdivided into

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elementary, relift and triple lift, these series differ in topology by the number of energy storage elements and their interconnections. This paper focuses on the additional series SEPOSLC with input side capacitor splitted to vary the voltage gain of the converter. High voltage converters are susceptible to external disturbances, to regulate the output voltage of SEPOSLC, a suitable controller has to be designed. Therefore, modeling of SEPOSLC is done using state-space averaging technique. Line side and load side regulation of the SEPOSLC is achieved by using PI Controller. Simulation is carried out using MATLAB/SIMULINK software. Hardware is built using analog components to elucidate the results.

The organization of the paper is as follows. Firstly, a explanations for the abbreviations used in the equations are discussed in section 2, a principle of operation of the split capacitor type elementary additional series positive output superlift Luo converter is discussed in section 3. Then state space averaging model of the converter is derived in section 4. In section 5 PI Controller of the converter is designed. Simulated and experimental results are shown.

2 Nomenclature

Table 1. Important terms in SEPOSLC Model

Term	Description	Term	Description
V_{in}	Input voltage	i_{C_2-off}	Current in the capacitor C_2 during OFF state
V_o	Output voltage	i_{C_3-off}	Current in the capacitor C_3 during OFF state
V_1	Voltage across the capacitor C_1	Δi_L	Ripple in the inductor current
K	Duty cycle	δi_L	Variation ratio of the inductor current
i_{in-off}	Input current during the OFF state	L	Inductance
i_{in-on}	Input current during the ON state	R	Resistance
i_{L-off}	Current in the inductor L during OFF state	C	Capacitance
i_{C_1-off}	Current in the capacitor C_1 during OFF state	f	Switching frequency
$i_{C_{11}-off}$	Current in the capacitor C_{11} during OFF state	C_{12}	Output capacitance
i_{C_1-on}	Current in the capacitor C_1 during ON state	ΔV_o	Ripple in the output voltage
i_{C_2-on}	Current in the capacitor C_2 during ON state	ΔQ	Change of charge accumulation
I_o	Output current	T	Time period
I_L	Average inductor current	δ_{V_o}	Variation ratio of the output voltage

3 Principle of operation of split capacitor type positive output super lift converter

3.1 Circuit description and operation

The circuit diagram of split capacitor type elementary additional series positive output super lift converter is shown in Fig. 1. It consists of DC supply voltage Vin, capacitors C_1 to C_3, C_{11}, C_{12} inductor L, switch S_1 and S_2, freewheeling diodes D_1 to D_7, D_{11}, D_{12} and load resistance R.

Figs. 2 and 3 shows the ON and OFF modes of operation of the converter under continuous conduction mode. Capacitor C_1 and C_2 are charged to V_{in} during the ON state of the switch under the steady state condition.

The inductor current i_L increases with voltage V_{in} during the switching-on period kT.

Inductor current iL decreases with voltage $-[V_O - V_1 - V_{in}]$ during switching-off period $(1-k)T$. The peak to peak current ripple in the inductor is the same during steady state operation and is given by

$$\Delta_{iL} = \frac{V_{in}}{L} KT = \frac{V_o - V_1 - V_{in}}{L}(1-k)T, \tag{1}$$

$$V_o = \left(\frac{1}{1-k} + \frac{3-2k}{1-k}\right) V_{in}. \tag{2}$$

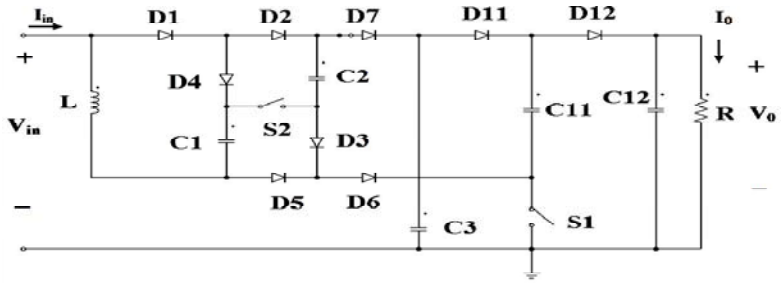


Fig. 1. Split capacitor type elementary additional series positive output super lift converter

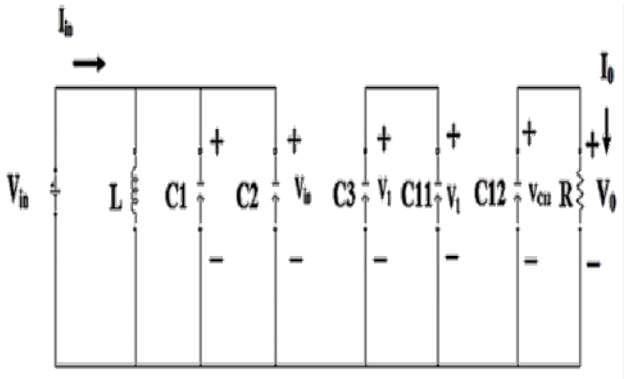


Fig. 2. ON Mode operation the inductor current i_L increases with voltage V_{in} during the switching-on period k_T

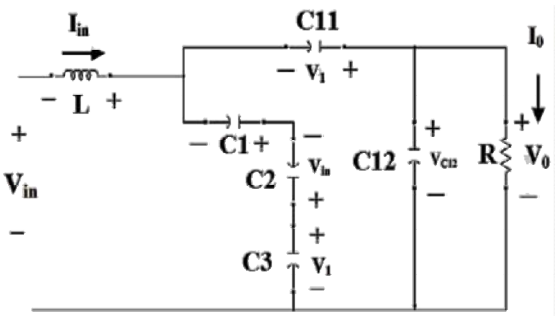


Fig. 3. OFF Mode operation

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k} + \frac{3-2k}{1-k}\right). \tag{3}$$

The input current i_{in} is equal to $(i_L + i_{C1} + i_{C2})$ during ON mode and only equal to i_L during switching-OFF. Capacitor current i_{C1} and i_{C2} is equal to i_{C3} during switching-OFF. At steady state, the voltage across the capacitor C_1, C_2 is equal to V_{in}. The following relations are obtained[6].

$$\begin{aligned} i_{in-off} &= i_{L-off} = i_{C1_off} + i_{C11-off}, \\ i_{in-on} &= i_{L-on} = i_{C1_on} + i_{C11-on}, \\ i_{C1-on} &= \frac{I_o}{k}. \end{aligned} \tag{4}$$

If inductance L_1 is large enough, i_L is nearly equal to its average current I_L . Therefore

$$\begin{aligned} i_{in-off} &= i_{C1-off} = i_{C11_o ff}, \\ i_{C1-off} &= i_{C2-off} = i_{C3_o ff}, \\ i_{in-off} &= I_L = \frac{2I_o}{1-k}, \\ i_{C1-off} &= I_{C2-off} = \frac{I_o}{1-k}. \end{aligned} \tag{5}$$

And average input current

$$I_{in} = k1_{in-on} + (1-k)i_{in-off} = \frac{4I_o}{1-k}. \tag{6}$$

The variation ratio of inductor current i_L is

$$\zeta_{iL} = \frac{\Delta i_{L/2}}{i_L} = \frac{k(1-k)^2 R}{8(4-2k)Lf}. \tag{7}$$

Ripple in the output voltage V_o is

$$\Delta V_o = \frac{\Delta Q}{C_{12}} = \frac{(1-k)TI_o}{C_{12}} = \frac{(1-k)V_o}{fC_{12}R}. \tag{8}$$

Therefore, the variation ratio of output voltage V_o is

$$\zeta_{V_o} = \frac{\Delta V_o/2}{V_o} = \frac{(1-k)}{2RfC_{12}}. \tag{9}$$

4 State space averaged model of split capacitor type positive output super lift converter

Modeling of converter can be done by circuit averaging and state space averaging technique. State space averaging is more advantages such as more compact representation of equations and ease in deriving the transfer functions. Write the state equations for each switched circuit model using basic laws and average the state space equation using the duty ratio. State variables X_1, X_2, X_3, X_4, X_5, X_6 are chosen as the current in the inductor i_{L1}, the voltage across the capacitor V_{C1}, V_{C2}, V_{C3}, V_{C11}, V_{C12} respectively[8]. From Fig. 2 during ON state, the state space equation is written as

$$\begin{aligned} X_1 &= \frac{U_1}{L}, \\ X_2 &= \frac{U_1}{R_{in}(C_1+C_2)} - \frac{X_1}{(C_1+C_2)}, \\ X_3 &= \frac{U_1}{R_{in}(C_1+C_2)} - \frac{X_1}{(C_1+C_2)}, \\ X_4 &= \frac{A \times U_1}{R_{in}(C_1+C_2)} - \frac{X_1}{(C_1+C_2)}, \\ X_5 &= \frac{B \times U_1}{R_{in}(C_1+C_2)} - \frac{X_1}{(C_1+C_2)}, \\ X_6 &= -\frac{X_6}{RC_{12}}. \end{aligned} \tag{10}$$

From Fig. 3 during the state of the switch is OFF the split capacitor type elementary additional series positive output super lift converter state space equation is given as

$$
\begin{aligned}
X_1 &= \frac{k \times U_1}{(1-k) \times L}, \\
X_2 &= \frac{X_1}{D \times (C_1 + C_{11})}, \\
X_3 &= \frac{X_1}{D \times (C_1 + C_{11})}, \\
X_4 &= E \times X_1, \\
X_5 &= F \times X_1, \\
X_6 &= -\frac{X_6}{RC_{12}},
\end{aligned} \tag{11}
$$

where the A, B, D, E, F are constants and defined as

$$
\begin{aligned}
A &= B = (3 - 2k/1 - k) \times (C_{11}/C_3), \\
C &= (3 - 2k/1 - k), \\
D &= 1/\left(C_1 + C_{11} \times (3 - 2k/1 - k)\right), \\
E &= 1/\left(C_2 + C_{11} \times (3 - 2k/1 - k)\right), \\
F &= (C_1 \times C)/(C_3 \times C_1 + C_{11} \times C_3 \times C).
\end{aligned} \tag{12}
$$

With state space averaging method[3], the split capacitor type elementary additional series positive output super lift converter state space averaged equation in X_1, X_2, X_3, X_4, X_5, X_6 matrix form is given as

$$
\begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{-k}{C_1+C_2} + D(1-k) & 0 & 0 & 0 & 0 & 0 \\ \frac{-k}{C_1+C_2} + E(1-k) & 0 & 0 & 0 & 0 & 0 \\ \frac{-Bk}{C_1+C_2} + F(1-k) & 0 & 0 & 0 & 0 & 0 \\ \frac{-Ck}{C_1+C_2} + C_1(1-k) & 0 & 0 & 0 & 0 & 0 \\ \frac{C_1 C_{11}(1-k)}{C_{12}} + D(1-k) & 0 & 0 & 0 & 0 & \frac{-1}{RC_{12}} \end{bmatrix} \times \begin{bmatrix} X_1 \\ X_2 \\ X_3 \\ X_4 \\ X_5 \\ X_6 \end{bmatrix} + \begin{bmatrix} \frac{2k}{l} \\ \frac{k}{R_{in}(C_1+C_2)} \\ \frac{k}{R_{in}(C_1+C_2)} \\ \frac{Bk}{R_{in}(C_1+C_2)} \\ \frac{Ck}{R_{in}(C_1+C_2)} \\ 0 \end{bmatrix} \times U_1, \tag{13}
$$

$$
V = AV + BU.
$$

Its output equation is given as

$$
V_o = V_{C12}, \tag{14}
$$

where R_{in} is internal resistance of source, u is input variable, k is duty cycle or the status of the switches, X_1, X_2, X_3, X_4, X_5, and X_6 are the vectors of the state variables (i_{L1}, V_{C1}, V_{C2}, V_{C3}, V_{C11}, V_{C12}) and their derivatives respectively.

5 Design of PI controller

PI controller fuses the properties of both P and I controller with zero steady state error. It is designed to regulate the split capacitor type elementary additional series positive output super lift converter against line side and load side variations, so that it stays very closer to the nominal operating point in the case of sudden disturbances and components variations.

Proportional gain (K_P) and integral time (T_i) constants are tuned using Zeigler-Nichols(ZN) method. Values of L and T are obtained from open loop characteristics of split capacitor type positive output super lift converter as shown in Fig. 4 with $L = 0.0002s$ and $T = 0.004s$. The delay time and time constant are determined by drawing a tangent line at the inflection point of the S-shaped curve and determining the intersections of the tangent line with the time axis and line output[2, 4]. The values of $K_P = 1.8$ and $T_i = 0.0066s$ are determine using ZN method. Fig. 5 shows the PI Controller simulation model in MATLAB / SIMULINK Software.

K_p and T_i are optimally tuned by finding the minimum values of integral of square of error (ISE), integral of time of square of error (ITAE) and integral of absolute of error (IAE) [5] which is listed in Tab. 2.

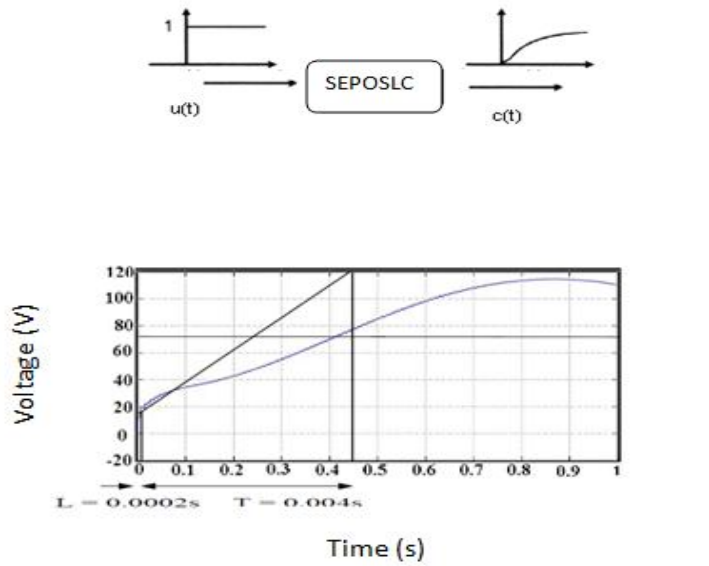


Fig. 4. Open loop characteristics of SEPOSLC

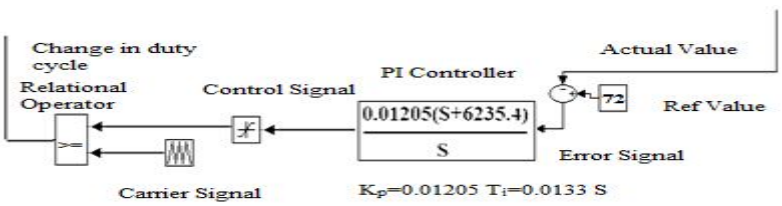


Fig. 5. PI controller simulation model in simulink

Table 2. Simulated results of minimum values of ISE, IAE, ITAE and optimal settings of K_p and T_i

ISE	IAE	ITAE	K_p	$T_i(s)$
0.00154	0.0154	0.3059	0.01205	0.0133

6 Simulation results

The performance of the converter is validated for five regions viz. transient region, line variations, load variations, steady state region and also for component variations. Simulations have been performed on the split capacitor type elementary additional series positive output super lift converter circuit with parameters listed in Tab. 3. The static and dynamic performance of the converter have been evaluated using MATLAB/SIMULINK software.

6.1 Transient region

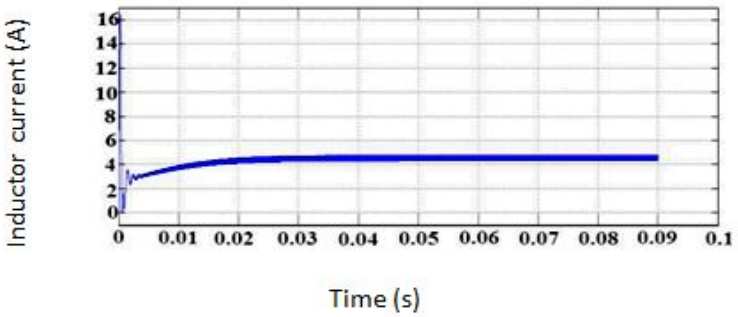
Fig. 6 shows the inductor current and output voltage of PI controlled SEPOSLC in the transient region. It can be viewed that the converter has a negligible overshoot and reaches a steady state at $0.037s$.

6.2 Line voltage variations

Line voltage of SEPOSLC is varied from $12V$ to $9V$ (-30% line disturbance) at $0.05s$. The output response of the converter is shown in the Fig. 7. It can be observed that the maximum overshoot is $16V$ and the steady state is reached within the $0.02s$ with proportional and integral gain chosen. Fig. 8 shows the step

Table 3. Parameters of split capacitor type elementary additional series positive output super lift converter

Parameters	Value
Input Voltage (V_{in})	12V
Output Voltage (V_o)	72V
Inductor (L)	100μH
Capacitors (C_1 to C_5)	30μF
Nominal switching frequency (f_s)	100kHz
Load Resistance (R)	50ω
Range of duty cycle (K)	0.3 to 0.9
Desired duty cycle K)	0.5



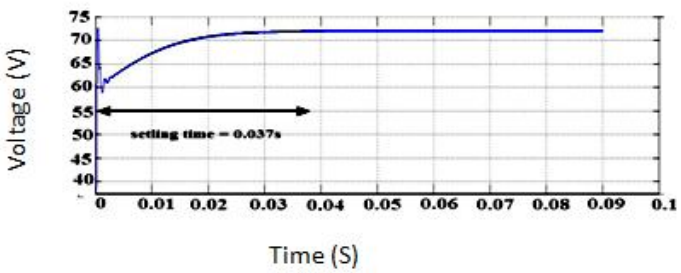


Fig. 6. Inductor current and output voltage in a transient region

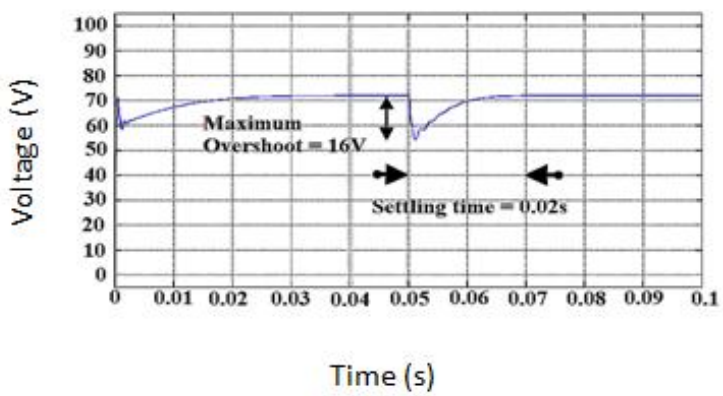


Fig. 7. Output response for a step decrease in the input voltage from $12V$ to $9V$

increase in the input voltage from $12V$ to $15V$ ($+30\%$ line disturbances) at $0.05s$. The maximum overshoot is $18V$ and the response reaches the steady state value at $0.03s$.

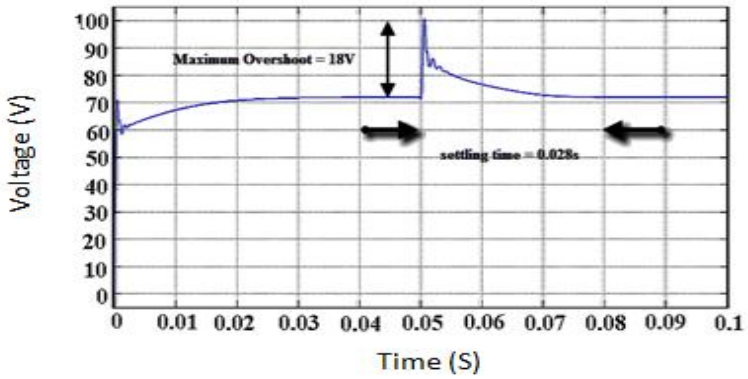


Fig. 8. Output response for a step increase in the input voltage from $12V$ to $15V$

6.3 Load impedance variations

For a step change in the load impedance from 50Ω to 60Ω as shown in the Fig. 9. The output response overshoots $0.5V$ and reaches the steady state value within $0.03s$. For a step decrease in load from 50Ω to 40Ω

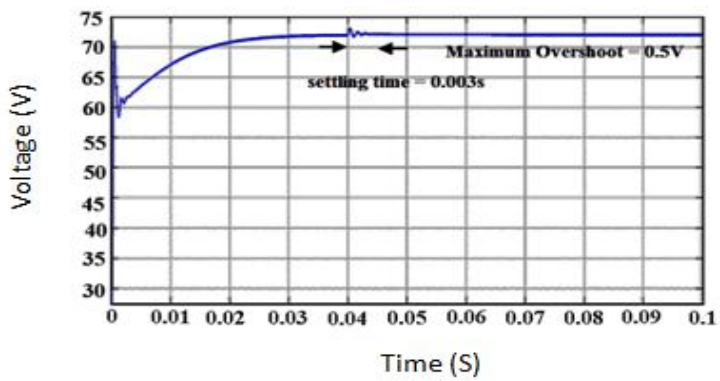


Fig. 9. Output voltage when load resistance makes a step changes from 50Ω to 60Ω

(-20% load disturbance) as shown in Fig. 10. It could be observed that there is a small overshoot of $0.5V$ and steady state is reached at $0.004s$.

6.4 Steady state region

Variation of the inductor current and output voltage at steady state is shown in the Fig. 11. It is observed that the ripple in the inductor current and the output voltage is of less value about $0.55A$ and $0.45V$.

6.5 Circuit components variations

Variation of inductor and capacitor value from $100\mu H$ to $300\mu H$ and $30\mu F$ to $120\mu F$ is shown in Figs. 12 and 13. It is observed that the output voltage as some peak overshoot and reaches the steady state value of $72V$.

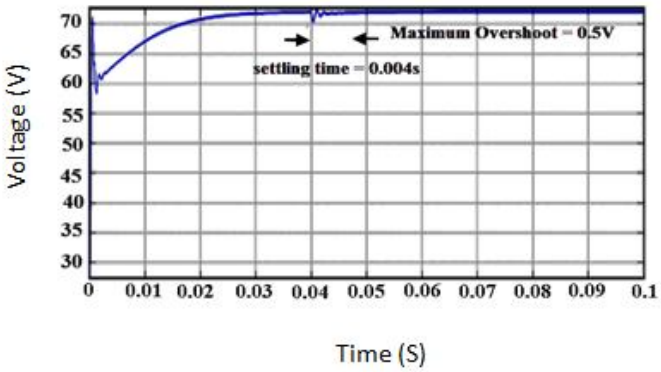


Fig. 10. Output voltage when load resistance makes a step changes from 50Ω to 40Ω

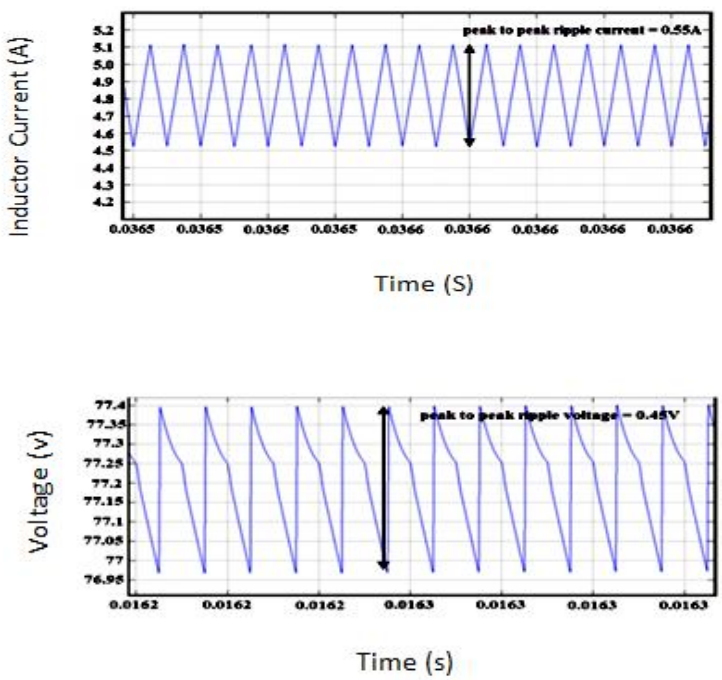


Fig. 11. Inductor current and output voltage variation at steady state

7 Hardware setup

The laboratory prototype of SEPOSLC was developed with the specified simulation circuit parameters with PI Controller. The laboratory prototype of SEPOSLC using the analog circuits is shown in Fig. 14. The power circuits components are as follows IRFN 540 (MOSFET)[1], D_1-D_9 FR306 (Diodes), $C_1 - C_6$ $30\mu F/10V$ (plain polyester type) capacitor, L_1 $100\mu H/5A$ (Ferrite Core) inductor, Decade resistance box is used to add the load of $50\Omega/2A$ and to vary the load resistance. Input side line variation is achieved by using variac. Gating pulses for the switches S1 and S2 are shown in the Fig. 15. Pulses are generated by using voltage comparison method to change the ON time of the switch with the frequency fixed. Pulse for switch S2 is obtained by inverting the pulse for switch S1 by using NOT Gate. The designed PI control is

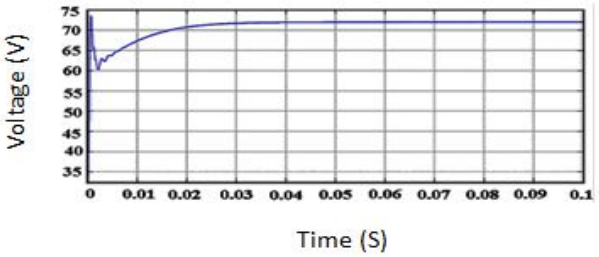


Fig. 12. Output voltage when capacitors are varied from $30\mu F$ to $120\mu F$

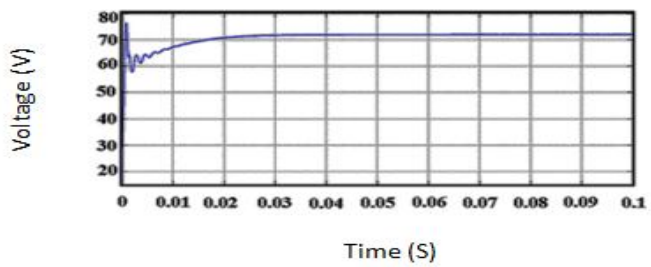


Fig. 13. Output voltage when inductor is varied from $100\mu H$ to $300\mu H$

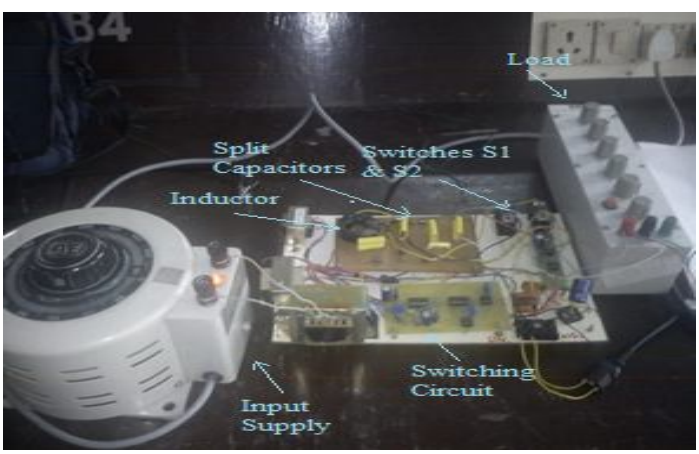


Fig. 14. Hardware prototype of SEPOSLC

implemented in an analog platform as shown in Fig. 16. and its operation is as follows; the inductor current and the capacitor voltages V_{c1} and V_{c2} of the SEPOSLC are sensed by using an feedback resistances, which are then compared with the reference signal by using an TL084 operational amplifier to generate error signal. Using TL084 PI controller is developed to reduce the steady state error. pulse width modulated signals are generated by comparing the output of the controller with the carrier signal generated by NE555 timer circuit. This pulsed output is passed through opto coupler (IR2125) and the driver circuit. The output of the driver is directly connected to the gate terminal of the MOSFET through the current limiting resistance. Using the PI control, the duty cycle of the gate pulse is varied to regulate the output voltage against the disturbances.

The output voltage response of a SEPOSLC for an input voltage of $12V$ at steady state is $72V$ as shown in Fig. 17.

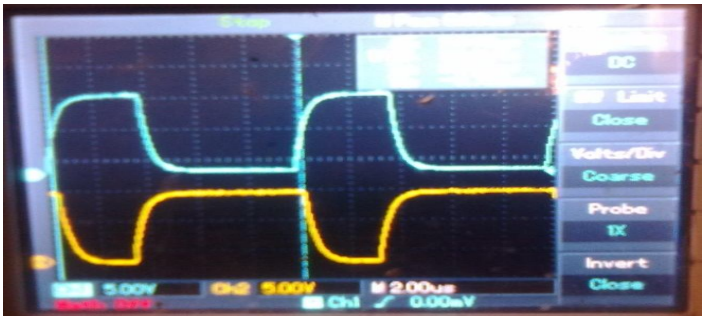


Fig. 15. Switches S1 and S2 Gating Pulses

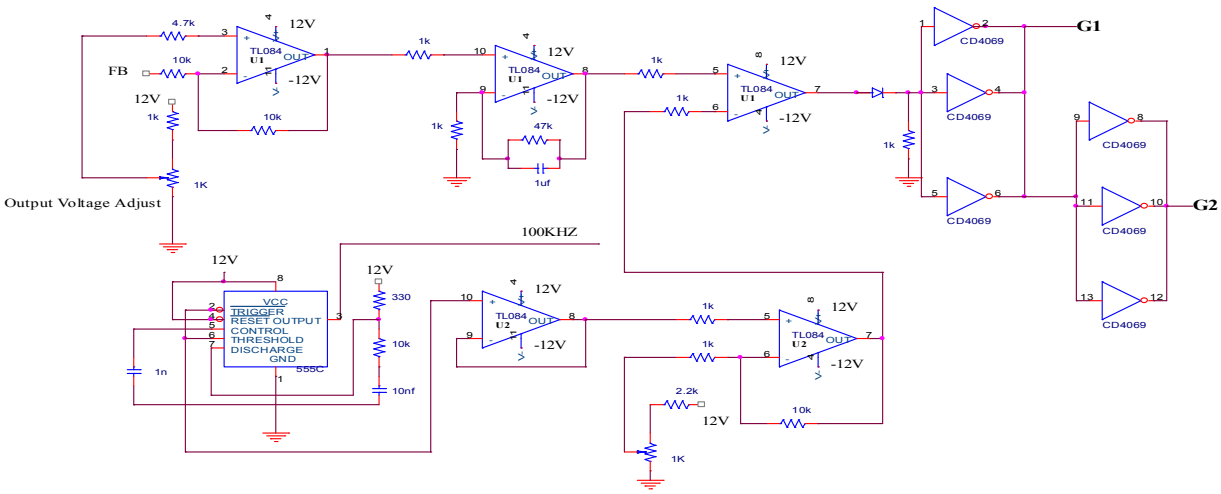


Fig. 16. Laboratory prototype model of SEPOSLC using PI control analog platform

Fig. 17. Output voltage response of SEPOSLC

7.1 Line voltage variations

Fig. 18 shows the line voltage variation of the SEPOSLC using the PI controller for an input voltage step change from $12V$ to $9V$ (-30% line variations) at time $= 0.05s$. The output response has a maximum overshoot of $0.5V$ and a settling time of $0.01s$.

A step increase in the input voltage from $12V$ to $15V$ ($+30\%$ line voltage disturbances) causes the output voltage to change and the designed PI Controller regulates the output voltage to $72V$ with the settling time less than $0.05s$ as shown in Fig. 19.

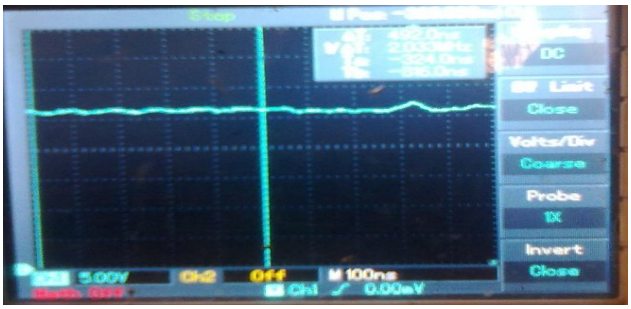


Fig. 18. Line voltage variation from $12V$ to $9V$

Fig. 19. Line voltage variation from $12V$ to $15V$

7.2 Load variations

Fig. 20 shows the output voltage of the SEPOSLC using the PI control for a step change in load resistance from 50Ω to 60Ω ($+20$ % load variations) at time$=$ $0.05s$. It can be seen that the peak overshoot is of $0.5V$ with a quick settling time of $0.01s$. A step decrease in load resistance from 50Ω to 40Ω (-20 % load variations) at time$=$ $0.05s$ causes the output voltage to vary from the steady state and the designed PI controller regulates the voltage to $72V$ with negligible overshoot as shown in Fig. 21.

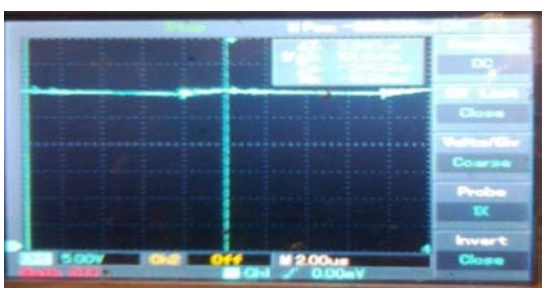


Fig. 20. Load variation from 50Ω to 60Ω at $0.05s$

8 Conclusions

This paper has presented the split of an input side capacitor of an converter to increase the voltage gain of the converter, design, analysis and suitability of PI controller for split capacitor type elementary additional series positive output super lift converter. The simulation based performance analysis of a PI controlled split capacitor type elementary additional series positive output super lift converter circuit has been presented along with its state space averaged model. The PI controller has been evaluated for transient region, line and load

Fig. 21. Load variation from 50Ω to 40Ω at $0.05s$

regulations, steady state region and also with circuit component variations and it is found that it proved to be robust. The only disadvantage of this converter topology in improving the voltage transfer gain is more number of capacitors, requirement of two switches and complimentary drive circuit.

References

[1] IRF540N datasheet. *International Rectifier Inc*.

[2] P. Comines, N. Munro. PID controllers : recent tuning methods and design to specification. *IEEE Proceedings Control Theory Application*, 2002, **149**(1): 46-53.

[3] Y. Jiao, F. Luo, M. Zhu. Generalized modelling and sliding mode control for n-cell cascade superlift DC-DC converters. *IET Power Electron*, 2011, **4**(5): 532–540.

[4] R. Kayalvizhi, S. Natarajan, A. Rosella. Design and simulation of PI controller for postive output elementary Luo converter. *Journal of Engineering and Technology, Annamalai University*, 2005, 90–93.

[5] K. Kumar, S. Jeevananthan. PI control for positive output elementary super lift Luo converter. *World Academy of Science, Engineering and Technology*, 2010, **63**: 732–737.

[6] F. Luo. Investigation on split capacitors applied in positive output super lift Luo converter. *Control and Decision Conference*, 2011, **2**792–2797.

[7] F. Luo, H. Ye. Advanced DC/DC converters. *CRC Press*.

[8] K. Ogata. Modern control engineering. *Prentice-Hall of India Private Limited*.

[9] Y. Tang, T. Wang, Y. He. A switched capacitor based active network converter with high voltage gain. *IEEE Transaction on power electronics*, 2014, **29**(6): 2959–2968.