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Hybrid 5-level inverter fed induction motor drive

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Abstract. Recently multilevel inverters (MLI) gained researchers interest due to efficient power conversion with multiple voltage steps resulting in improved power quality, reduced switching losses, higher electromagnetic compatibility and better voltage capability. This paper presents a three phase five level hybrid H-bridge inverter for effective control of induction motor drive. Space Vector Pulse Width Modulation (SVPWM) control scheme is proposed for the hybrid H-bridge multilevel inverter fed induction motor drive. The implementation of the SVPWM technique to Hybrid MLI was simulated in MATLAB/ Simulink environment and its results are presented.

Keywords: Hybrid Multi Level Inverter (MLI), H-bridge, SVPWM technique, THD

1 Introduction

Multilevel inverters include an array of power electronic devices and voltage sources with shunt capacitances, the output of which are voltages generated in the form stepped waveforms. The commutation of the switches provides the addition of the capacitor voltages, thus reaching high voltage at the output, while the power devices must withstand only reduced voltages[8].

These multilevel inverters (MLI) have become an effective solution for increasing power and reducing harmonics of AC waveform [7]. It involves the concept of utilizing a large number of active semiconductor switches to perform the power conversion in small voltage steps for higher voltage and reduction in harmonic distortion.

Three different topologies have been proposed for multilevel inverters: diode-clamped, flyback capacitors and cascaded H-bridge inverters In addition, several control strategies have been developed for multilevel inverters including the following: Space Vector Pulse Width Modulation (SVPWM)[3]. Among the various topologies of the multilevel inverters; cascaded H-bridge and the Hybrid inverter for 5-level requires two independent DC sources. The number of switches used for cascaded five level inverter is 8 where as hybrid H Bridge topology requires only 6 switches with 2 capacitors. Several PWM methods have been developed for the multilevel inverter designs[4]. Analytical solutions of PWM strategies for multilevel inverters are used to identify that alternative phase opposition disposition PWM for diode-clamped inverters produces the same harmonic performance as phase-shifted carrier PWM for cascaded inverters, and hybrid PWM for hybrid inverters, when the carrier frequencies are set to achieve the same number of inverter switch transitions over each fundamental cycle[6].

Using this understanding, a PWM method is developed for hybrid H bridge inverters to achieve the same harmonic gains as phase disposition PWM achieves for diode-clamped topology.

Three-phase induction motors are most widely used due to robust construction and higher efficiency for industrial applications. Conventionally, DC machines were the work horses for the Adjustable Speed Drives

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(ASDs) due to their excellent speed and torque response[1]. But they have their own disadvantages like commutator design and brushes, which undergo wear and tear problems. Thus AC motors are preferred over dc motors due to its lesser cost, lower maintenance, low weight and higher efficiency rate.

The most attractive features of multilevel inverters are as follows[2].

- Can generate output voltages with extremely low harmonics or distortions.
- MLIs draw low input current with pretty low distortion.
- These generate smaller common-mode voltage (CMV), thus reducing the stress on the motor bearings.
- Usage of certain modulation techniques can eliminate CMV[5].
- MLIs can operate even with a lower switching frequency.

In this paper a three-phase hybrid five level inverter is developed by suitably modifying a conventional cascaded H-bridge inverter. The proposed topology reduces the number of power semiconductor switches. A Modified SVPWM technique is developed for generating the gating pulses to produce low harmonic distortion and effective voltage levels.

2 Proposed topology

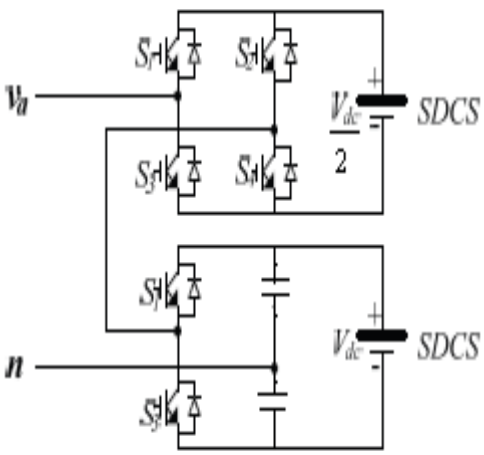

Fig. 1. Single-phase 5-level hybrid inverter

The main circuit of a single-phase 5-level Hybrid MLI is shown in the Fig. 1, includes a standard one leg inverter with a separate dc power source connected in series with a single H-bridge inverter. In this topology the four-switch inverter is referred to as main inverter and the two-switch H-bridge inverter as auxiliary inverter. Low switching losses occur during PWM mode, the main inverter will operate on square wave mode and the auxiliary inverter will operate on PWM mode. In modified PWM technique the reference wave is a combination of both sine and triangular wave and it is compared with a carrier triangular wave then the gate pulses are generated.

2.1 Cascaded H-bridge 5-level inverter

Fig. 2 illustrates the circuit configuration of a cascaded H-bridge 5-level inverter. The each phase has its own dc sources. A separate dc source is connected to each leg of an H-bridge inverter. The number of output-phase voltage levels is defined by $m = 2N + 1$, where N is the number of DC sources. The number of switches used in this topology are $N_{switch} = 4s$, where N is the number of dc sources.

The 5-level cascaded H-bridge MLI consists of two H-bridges in each phase. The first H-bridge output voltage is denoted by V_1 and the output of the second H-bridge is denoted by V_2, so that the output voltage of the cascaded multilevel inverter is the sum of the two voltages $V_0 = V_1 + V_2$ by appropriate opening and

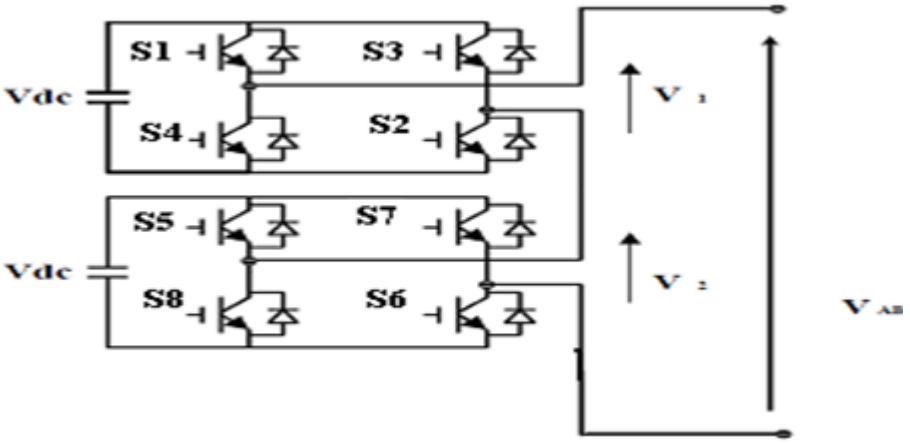

Fig. 2. Three-phase cascaded H-bridge 5-level inverter

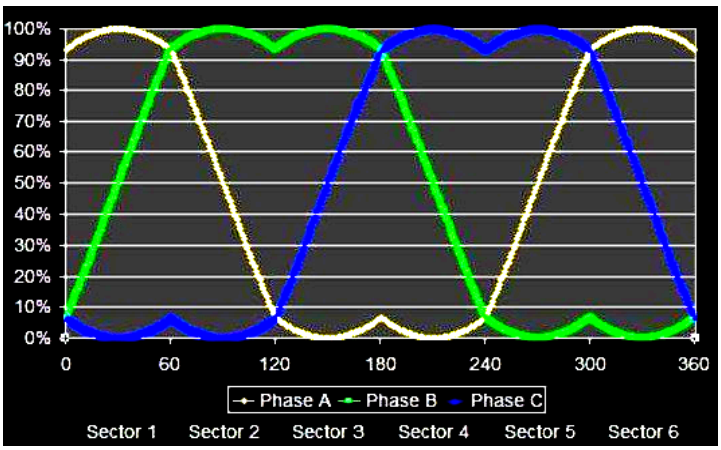

Fig. 3. Generation of SVPWM pulses

closing of the switches of H1 the output voltage V_1 can be made equal to $+V_{dc}/2$, 0, $-V_{dc}/2$ while the output voltage of H_2 can be made equal to $-V_{dc}/2$, 0, $+V_{dc}/2$. Therefore the output voltage of the inverter is a combination of $V1$ and V_2 as shown in Table 2, the five possible values are $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$.

Space Vector Pulse width Modulation (SVPWM) generates the appropriate gate drive waveform for each PWM cycle. The inverter is treated as one single unit and can combine different switching states (number of switching states depends on levels). The SVPWM provides unique switching time calculations for each of these states. This technique can easily be changed to higher levels and works with all kinds of multilevel inverters (cascaded, capacitor clamped, diode clamped). The three vectors that form one triangle will provide duty cycle time for each, giving the desired voltage vector (Vref). This can be described with the formula: $V = T_1V_1 + T_2V_2 + T_3V_3/T_c$. The Simulink model to generate the SVPWM pulses is shown in Fig. 3. The cascaded 5 level output voltage waveform is shown in Fig. 4.

2.2 Hybrid 5-level inverter

The main circuit configuration of the proposed hybrid H-bridge multilevel inverter is shown in Fig. 5, which includes a complete and a simplified single-phase topology. This structure includes a standard 3-leg inverter (one leg for each phase) with a dc power source (V_{dc}) and H-bridge in series with each inverter leg with a separate dc source $+V_{dc}/2$ in other words The hybrid 5-level inverter consists of a three-phase inverter and a three h-bridge inverters.

The output voltage V_1 of this leg is either $+V_{dc}/2$ when closed or $-V_{dc}/2$ when Ga6 closed. This leg is connected in series with a full H-bridge inverter, then the output voltage V2 of the H-bridge inverter is either

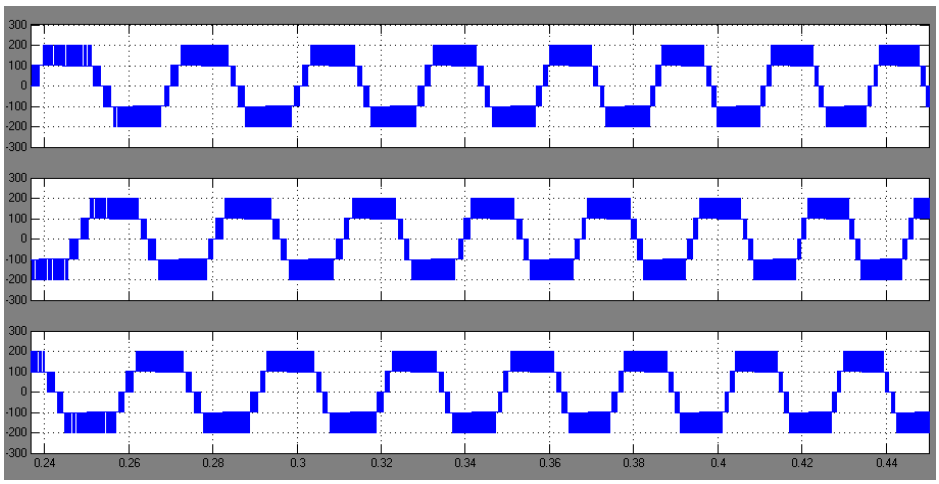

Fig. 4. Cascaded Five-level output voltage wave form

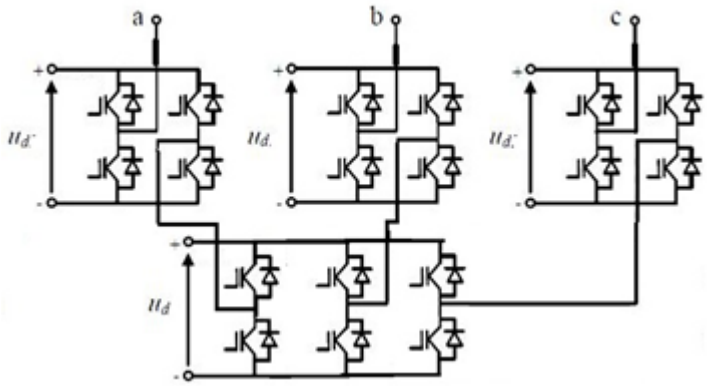

Fig. 5. Three-phase cascaded Hybrid 5-level inverter

$+V_{dc}/2$ when G_{a1}, G_{a2} are closed, 0 when G_{a1}, G_{a3}, or G_{a2}, G_{a4} closed, or $-V_{dc}/2$ when G_{a3}, G_{a4} closed. Switching pattern in one leg of the cascaded Hybrid 5-level inverter is given in Tab. 1. When the output voltage $V_0 = V_1 + V_2$ is required to be zero, one can either set $V_1 = +V_{dc}/2$ and $V_2 = -V_{dc}/2$ or $V_1 = -V_{dc}/2$ and $V_2 = +V_{dc}/2$.

Table 1. Switching States in One Leg of the Cascaded Hybrid Five-Level Inverter

S. No.	Voltage levels	On switches
1	0	G_{a1}, G_{a2}, G_{a6}
2	$\frac{+V_{dc}}{2}$	G_{a1}, G_{a3}, G_{a5}
3	$+V_{dc}$	G_{a1}, G_{a2}, G_{a5}
4	$\frac{-V_{dc}}{2}$	G_{a1}, G_{a3}, G_{a6}
5	$-V_{dc}$	G_{a3}, G_{a4}, G_{a6}

3 Results

The three-phase Hybrid H-bridge five level inverter fed induction motor is simulated and the corresponding five level output voltage wave forms with SVPWM technique are shown in Fig. 6 and Fig. 7. Its corresponding output current, torque; speed curves with respect to time are shown in Fig. 8, Fig. 9 and Fig.

10 respectively. The THD of a Hybrid 5-level inverter using with and without Modified PWM technique is shown in Fig. 11.

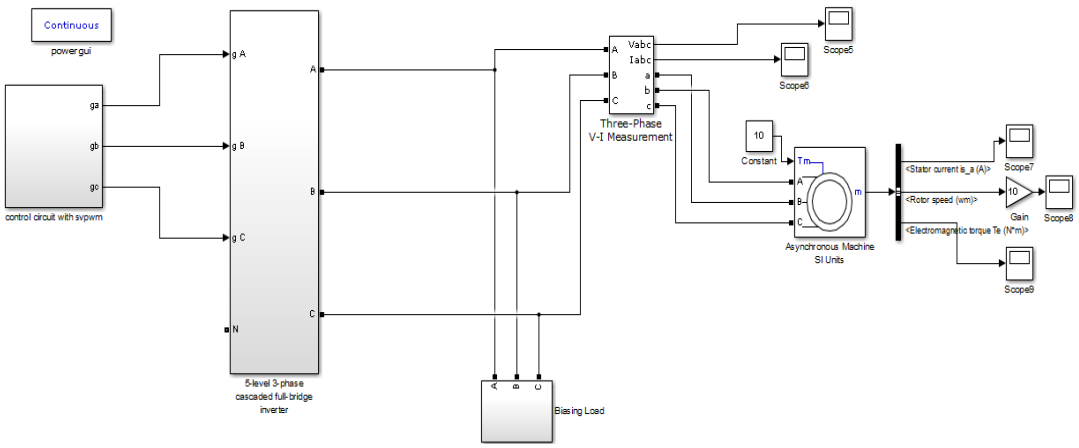

Fig. 6. Simulink model of Hybrid MLI using SVPWM technique

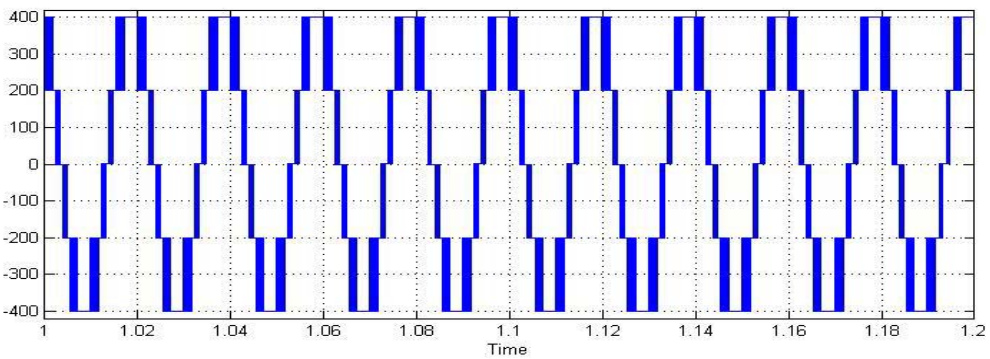

Fig. 7. Output voltage waveform of the Hybrid H-bridge inverter with SVPWM technique

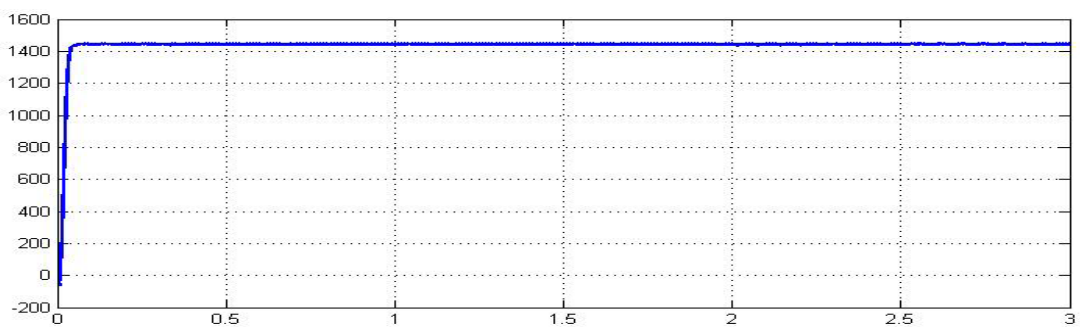

Fig. 8. Speed curve of a three-phase induction motor w.r.t time

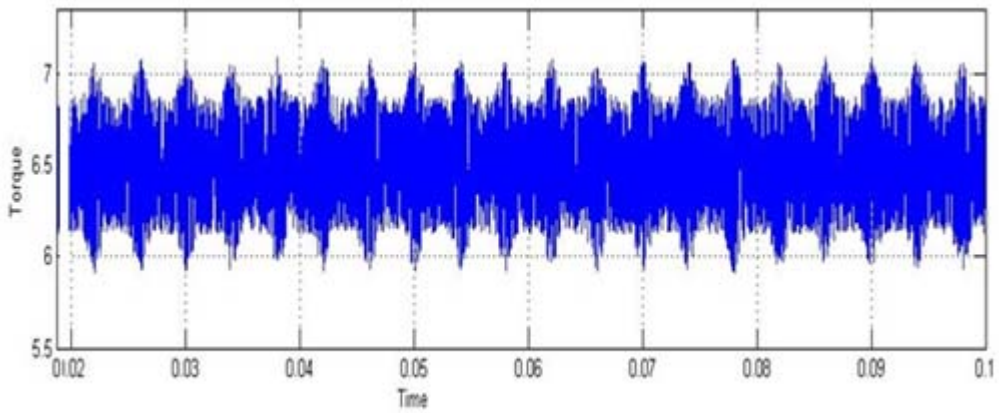

Fig. 9. ElectroCMagnetic torque w.r.t time of a three-phase induction motor.

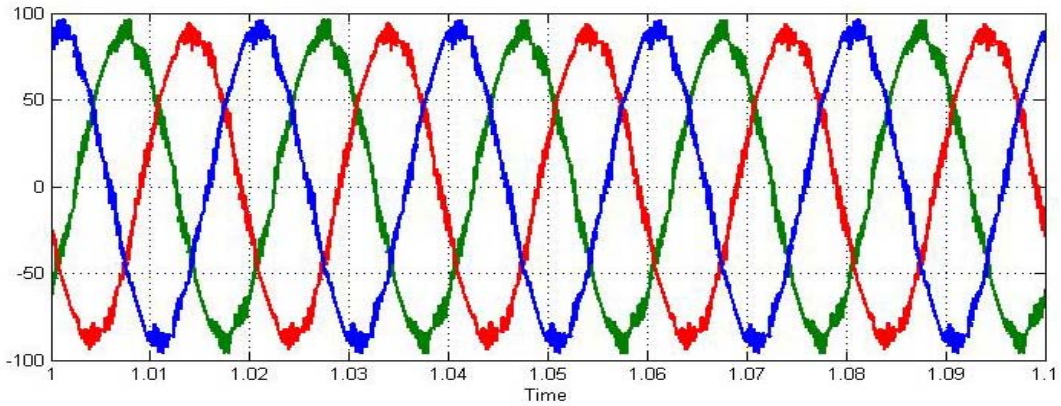

Fig. 10. Output current waveform of a cascaded hybrid 5-level inverter fed induction motor.

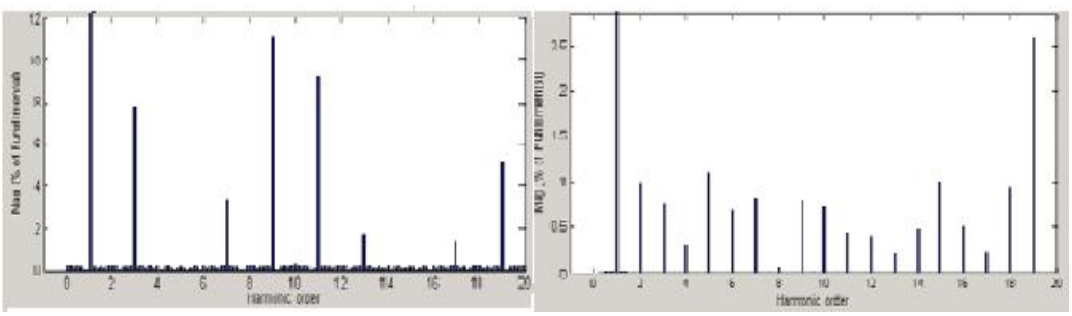

Fig. 11. THD of a Hybrid 5-level inverter with and without SVPWM technique

4 Conclusion

A three-phase Hybrid five level inverter fed induction motor drive is presented in this paper and observed the performance characteristics of the motor with SVPWM technique. The SVPWM technique and its output spectra were calculated from basic operation and then simulated using MATLAB. The simulation results show reduced switching losses and total harmonic distortion. It is also observed that the proposed topology decreased the number of required power electronic switches compared to a cascaded H-bridge inverter to obtain the same five level output voltage with lower THD. The induction motor performance curves such as speed, torque and current are presented. The simulation results show that the hybrid H-bridge fed Induction Motor drive has a satisfactory performance.

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