

Space vector pulse width modulation of three-phase DCMLI with neuro-fuzzy MPPT for photovoltaic system

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Abstract. This paper presents a control for a three-phase seven-level diode-clamped multilevel inverter (DCMLI) for photovoltaic (PV) systems which improves DC link utilization, output voltage quality and avoids the DC link capacitor voltage balancing problem experienced with standard multilevel operation. The maximum power point tracking (MPPT) is capable of extracting maximum power from PV array connected to each DC link voltage level and it is solved by neuro-fuzzy controller (NFC). Space vector pulse width modulation (SVPWM) algorithm uses a simple mapping to generate gate signals for the inverter. The control system employs the proportional controller (PI) controller to generate the SVPWM signals for IGBT switching, thus producing and regulating the 50Hz sinusoidal AC output voltage and to achieve high dynamic performance with low total harmonic distortion (THD). The validity of the system is verified through MATLAB/Simulink and the results are compared with three-phase three-level and five-level DCMLI for PV system in terms of THD. Finally, simulation results are presented to verify the effectiveness and accuracy of the proposed system.

Keywords: photovoltaic (PV) system, diode-clamped multilevel inverter (DCMLI), space vector pulse width modulation (SVPWM), total harmonic distortion (THD)

1 Introduction

With increasing concern about possible energy crisis and environmental issues, people have recognized the big potential of renewable energy resources. Therefore, many countries are actively developing electricity generation systems using renewable energy sources. An inherent feature of all renewable energy sources is the available energy varies randomly, resulting in a wide variation in the available output voltage and power that makes power converter, a necessary part of all such generation systems. The input of the converter in renewable generation can be either varied low DC voltage (eg. photovoltaic array) or AC voltage with wide variation of both amplitude and frequency (eg. wind generator)^[1].

Recently, the installation of photovoltaic (PV) generation systems is rapidly growing due to concerns related to environment, global warming, energy security, technology improvements and decreasing costs. PV generation system is considered as a clean and environmental-friendly source of energy^[2]. Different types of multilevel inverter (MLI) topologies like diode clamped multilevel inverter (DCMLI), flying capacitor MLI (FCMLI) and cascaded H-bridge MLI (CHMLI) are presented^[3]. Many methods of pulse width modulation (PWM) techniques are used to control the inverter including selective harmonic elimination PWM, sinusoidal PWM, space vector PWM, and similar variations of the three main algorithms^[4]. A novel simplified multilevel space vector modulation scheme based on two-level inverter geometry based on-time equations. The on-time calculation equations for various modulation mode do not change with the position vector like the traditional approach in [5].

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A single phase MLI can be controlled using phase shifted PWM as a feasible multi-string topology for PV applications. This topology can inject to the grid sinusoidal input currents with unity power factor, even under conditions of unequal solar radiation of the string of PV cells^[6]. In a PV system, proportional integral (PI) controller current control scheme is used to maintain the output current sinusoidal and to get high dynamic performance from the different atmospheric conditions. The novel PWM control scheme involves two reference signals identical to each other with an offset equivalent to the amplitude of the triangular carrier signal are used to generate PWM signal for the switches and to maintain the power factor unity^[7]. The scheme is^[8] proposed for a single-phase CHMLI for PV applications with fuzzy logic control and system-on-chip approach. The main contributions of this scheme use of fuzzy logic control with intermediate optimal PWM switching angle generator and PI controller. The modelling and simulation of three-phase five-level DCMLI using Sinusoidal PWM for grid connected PV system with fuzzy maximum power point tracking (MPPT) controller in [9]. In this scheme, the reduction of harmonics distortion is not enough to attain the effectiveness of the controller.

The total harmonic distortion (THD) minimization of the output voltage of multilevel inverters is discussed^[10]. In this approach, the fundamental frequency switching strategy, the switching angles can be selected so that the output THD is minimized. To obtain the optimum switching angles, an optimization algorithm is applied to the output voltage THD. Real time algorithm for minimizing THD in multilevel inverters, with unequal or varying voltage steps under staircase modulation^[11]. This algorithm results minimum THD of the output voltage of the inverter, which proved by rigorous mathematical derivations.

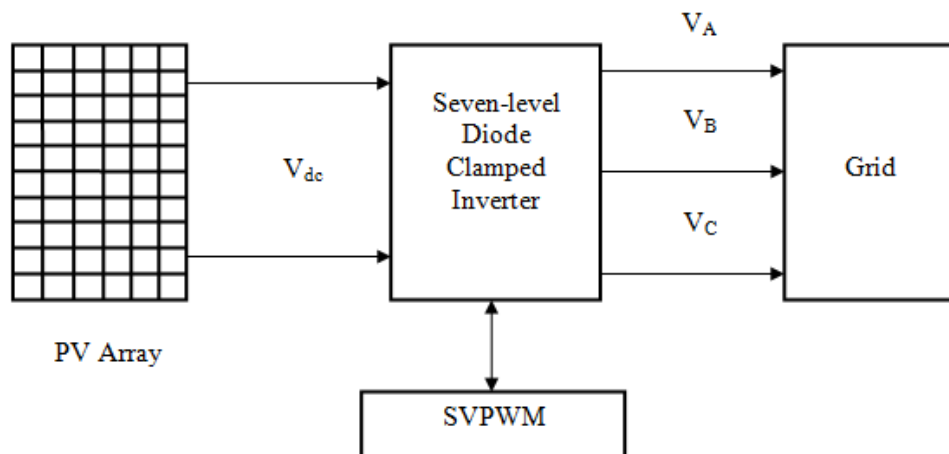


Fig. 1. General diagram of proposed system

In this proposed work, the main contribution is to reduce the THD at output voltage of the DCMLI for PV system and its control strategies. The whole system is simulated under standard atmospheric conditions (1000 W/m^2 , 25°C) in MATLAB and the irradiance is varied from 800, 600 and 1000 W/m^2 at a time period of 0 second, 0.08 seconds and 0.15 seconds respectively. This paper focuses on the development of a PV array connected to the three-phase multilevel DCMLI through DC bus which is connected to the three-phase load as shown in Fig. 1. The control structure of the proposed system is composed of two structure control. First, is the MPPT control, whose main property is to extract the maximum power from the PV generator and second is the inverter control is used to control DC bus voltage, to convert DC input to AC output at the same waveforms as the three-phase lines and to ensure high quality of the output power. This paper is organized as follows. In Section 2, the PV array modeling and simulation are described. In Section 3, MPPT control for the PV system. In Section 4, three-phase seven-level diode-clamped inverter topology has been presented. In Section 5, SVPWM algorithm has been presented, to confirm the effectiveness of the inverter control method. In Section 6, simulation result and discussion are presented. Finally, conclusions are given in Section 7.

2 Pv array modeling and simulation

The PV array used in the proposed system is shown in Fig. 1. The PV array used in the proposed system is KC200GT and it is simulated using a model based on [12]. In this model, a PV cell is represented by a current source in parallel with diode and a series resistance as shown in Fig. 2. In this PV array, mathematical model can be expressed as

$$I = I_{Photo} - I_{RSat} \left\{ \exp \left[\frac{q}{A_D K_B T} (V + I R_{Se}) \right] - 1 \right\} - \frac{V + R_{Se} I}{R_P}. \tag{1}$$

Eq. (1) shows that the non-linear output characteristics of solar cell. It is affected by temperature, radiation of solar and condition of load, where I_{Photo} is the photo current, I_{RSat} is the reverse saturation current, q is the electronic charge ($1.60217646 \times 10^{-19}$) and R_{Se} is the series resistance and R_p is the parallel resistance. Photocurrent I_{Photo} is directly proportional to the solar irradiation (G_{ira}). In Eq. (1) A_D is dimensionless factor, K_B is the Boltzmann constant ($1.38 \times 10^{-23} \text{ J/K}$) and T is the temperature. where I_{SC} short circuit current depends linearly on cell temperature and G_{iras} is the standard irradiation (1000 W/m^2).

$$I_{SC}(T) = I_{SCSat} [1 + \Delta I_{SC}(T - T_{St})], \tag{2}$$

where ΔI_{SC} is the temperature coefficient and T_{St} is the standard temperature (298K). I_{Photo} and I_{RSat} depend on the cell temperature and solar irradiation and these can be mathematically expressed as

$$I_{Photo}(G_{ira}, T) = I_{SCSat} \left(\frac{G_{ira}}{G_{iraS}} \right) [1 + \Delta I_{SC}(T - T_{St})], \tag{3}$$

$$I_{RSat}(G_{ira}, T) = \frac{I_{Photo}(G_{ira}, T)}{e^{\left(\frac{V_{oc}}{V_t}\right)} - 1}. \tag{4}$$

In Eq. (4), V_t is thermal voltage.

$$I_{photo}(G_{ira}) = I_{SC} \left(\frac{G_{ira}}{G_{iraS}} \right), \tag{5}$$

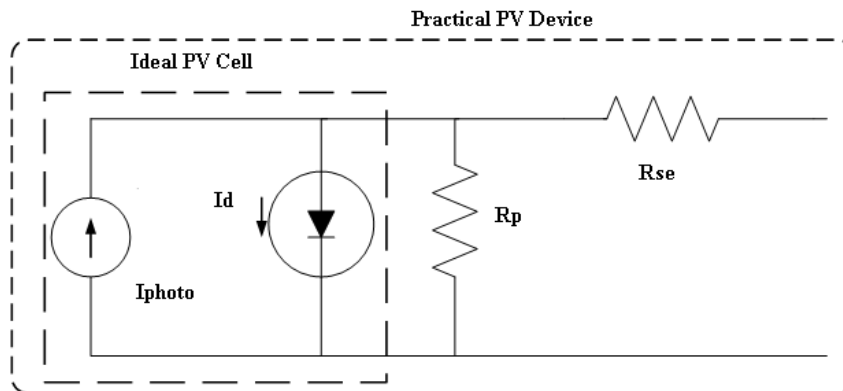


Fig. 2. Equivalent circuit of a PV cell physical model

3 MPPT control

Neuro-Fuzzy controller (NFC) is an intelligent control method combining the features of fuzzy logic controller (FLC) and artificial neural network (ANN). NFC is associated to an MPPT in order to improve

energy conversion efficiency under different environment conditions. To control a switch of the multilevel inverter, neuro-fuzzy MPPT control is used. It can deal with imprecise inputs, does not need an accurate mathematical model and can handle non-linearity. Therefore, NFC shows features of a nonlinear controller that has abilities such as learning, adaptation and making interference. The first stage of neural network is used, to estimate the optimal array voltage variation with solar isolation and cell temperature. FLC generating a control signal based on the voltage generated by the MPPT and the PV panel. Neural networks have learning and teaching algorithms, data collected through observation of PV panel different isolation and cell temperature. The collected data are used as training and updating neural parameters. The network training is performed repeatedly until the performance indexes; reduce below a specified value ideally to zero using Eq. (6),

$$E_p = (V_{ref} - V_{PV})^2. \quad (6)$$

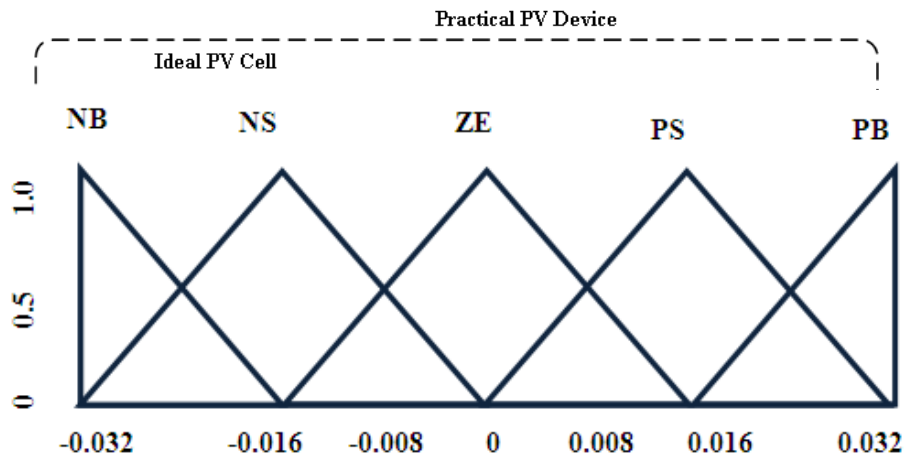


Fig. 3. Fuzzy input and output membership function

In other words, when E_p tends to zero and leads to $(V_{ref}CV_{PV})^2$ tends to zero, and then the trained neural network connecting weights are adjusted in such a way that the estimated array voltage is identically equal to the MPP voltage.

The fuzzy logic consists of three stages: fuzzification, interference system and defuzzification. Fuzzification comprises the process of numerical crisp inputs in to linguistic variables based on the degree of membership to certain sets. The seven fuzzy levels are used: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium) and PB (Positive Big). The partition of fuzzy subsets and the shape of membership function adapt the shape up to appropriate system. The value of input error (E) and the change in the error (ΔE) are normalized by an input scaling factor shown in Fig. 3. In this system the input scaling factor has designed such that input values are between -0.032 and 0.032. The triangular shape of the membership function of this arrangement presumes that for any particular input there is only one dominant fuzzy subset. FLC depend on shape of membership functions and rule base based on [13]. The inputs of the fuzzy controller are usually an error (E) and the change in the error (ΔE). The error can be chosen as $\Delta P / \Delta V$ because it is zero at the maximum power point. Then E and ΔE are defined as given in Eq. (7) and Eq. (8),

$$E = \frac{P(k) - P(k-1)}{V(k) - V(k-1)}, \quad (7)$$

$$\Delta E = E(k) - E(k-1). \quad (8)$$

The fuzzy rule base is the rules for three-phase inverter, where inputs are E and ΔE . The output is a change in the DC-link voltage (ΔV_{dc}). The interference system of this paper Max-Min method is used. The

membership function of each rule is given by the minimum operator and maximum operator. The defuzzification is used to convert from linguistic variable to a numerical crisp one again using membership functions as in Fig. 3. To compute the output of the FLC, centre of gravity method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch the inverter. It can be seen that the NFC tracks the operating point very quickly and faster than other MPPT techniques.

4 Three phase seven-level diode-clamped inverter topology

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of DC voltages, typically obtained from capacitor voltage sources. As the number of level increases, the synthesized output waveform has more steps, which produce a staircase wave the approaches, a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases. An n -level inverter consists of $(n - 1)$ capacitors on the DC bus and produces n -levels on the phase voltage. An n -level inverter leg requires $2(n - 1)$ switching devices, $(n - 1)$ capacitors and $(n - 1)(n - 2)$ clamping diodes.

In three-phase seven-level DCMLI, each of the three-phases of the inverter shares a common DC bus, which has been subdivided by six capacitors into seven levels. The voltage across each capacitor is V_{dc} , and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. Tab. 1 lists the output voltage levels possible for one phase of the inverter with negative DC rail voltage V_0 as a reference. State condition ‘1’ means the switch is ON and ‘0’ means the switch is OFF. Each phase has six complementary switch pairs such that turning ON one of the switches of the pair require that the other complementary switch be turned OFF. The complementary switch pairs for phase leg a are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, $(S_{a4}, S_{a'4})$, $(S_{a5}, S_{a'5})$ and $(S_{a6}, S_{a'6})$. For seven-level inverter, a set of six switches is ON at any given time. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage (V_{ab}) is a staircase waveform. This means that an n -level diode-clamped inverter has an n -level output phase voltage and a $2(n - 1)$ level output line voltage.

Table 1. DCMLI voltage levels and switching states

Voltage (V_a)	Switch						state					
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$	$S_{a'5}$	$S_{a'6}$
$V_6=6V_{dc}$	1	1	1	1	1	1	0	0	0	0	0	0
$V_5=5V_{dc}$	0	1	1	1	1	1	1	0	0	0	0	0
$V_4=4V_{dc}$	0	0	1	1	1	1	1	1	0	0	0	0
$V_3=3V_{dc}$	0	0	0	1	1	1	1	1	1	0	0	0
$V_2=2V_{dc}$	0	0	0	0	1	1	1	1	1	1	0	0
$V_1=1V_{dc}$	0	0	0	0	0	1	1	1	1	1	1	0
$V_0=0V_{dc}$	0	0	0	0	0	0	1	1	1	1	1	1

Although each active switching device is required to block only a voltage level of V_{dc} , the clamping diodes require different ratings for reverse voltage blocking. Using phase a as an example, when all the lower switches $S_{a'1}$ through $S_{a'6}$ are turned on, D_5 must block six voltage levels, or $5V_{dc}$. Similarly, D_4 must block $4V_{dc}$, D_3 must block $3V_{dc}$, D_2 must block $2V_{dc}$ and D_1 must block V_{dc} . If the inverter is designed such that, each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series. Consequently, the number of diodes required for each phase would be $2(n - 2)$. Thus, the number of blocking diodes is quadratically related to the number of levels in DCMLI. The switching sequence for seven-level DCMLI is listed in Tab. 1.

5 SVPWM algorithm

In this paper, space vector pulse width modulation (SVPWM) technique is used to generate PWM control signals to the inverter. Modulation index (MI) is defined as in Eq. (9)

$$MI = \frac{V_{P1}}{V_{P1SLX}}. \quad (9)$$

In Eq. (9), V_{P1} is the peak value of fundamental voltage and V_{P1SLX} is the peak value of fundamental voltage at six step operation. For a n -level cascaded topology $V_{P1SLX} = (2/\pi)(n-1)V_{dc}$, where V_{dc} is the dc link voltage. For a NPC topology $V_{P1SLX} = (2/\pi)(V_{dc})$, this is same as two-level inverter. The SVM is used to compensate the required volt-seconds using discrete switching states and their ON-times produced by inverter.

In a two level inverter, ON-time calculation is based on the location of reference vector within a sector S_i , $i = 1, 2, \dots, 6$. For a two-level inverter, volt-second equation is

$$V^Z T_S = V_X T_a + V_Y T_b. \quad (10)$$

The volt-seconds in terms of components V^Z , V_X and V_Y of along $\alpha - \beta$ axis are

$$V_\alpha^Z T_S = T_a + 0.5T_b, \quad (11)$$

$$V_\beta^Z T_S = hT_b, \quad (12)$$

$$T_S = T_a + T_b + T_0. \quad (13)$$

Solving Eq. (11), Eq. (12) and Eq. (13), obtain for the calculation of ON-times,

$$T_a = T_S \left[V_\alpha^Z - \left(\frac{V_\beta^Z T_S}{2h} \right) \right], \quad (14)$$

$$T_b = T_S \left[\frac{V_\beta^Z}{h} \right], \quad (15)$$

$$T_0 = T_S - T_a - T_b. \quad (16)$$

In Eq. (14), Eq. (15) and Eq. (16), h is height of the triangle of sector S_i $h = 0.866$ or $(\sqrt{3}/2)$, assuming that the sides of the equilateral triangle are unity. In Eq. (13), Eq. (14) and Eq. (15), $T_S = 1/(2f_s)$, f_s is the switching frequency. Each sector can be split into $(n-1)$ triangles, where n indicates level of the inverter. For any given reference vector, the sector of operation and its angle within the sector is determined by using Eq. (17) and Eq. (18), respectively.

$$S_i = \text{int} \left(\frac{\theta}{60} \right) + 1, \quad (17)$$

$$\gamma = \text{rem} \left(\frac{\theta}{60} \right), \quad (18)$$

where, $\theta(0^\circ \leq \theta \leq 360^\circ)$ is the angle of the reference vector with respect to α axis, $\gamma(0^\circ \leq \gamma \leq 60^\circ)$ is the angle within the sector and S_i ($1 \leq S_i \leq 6$) is its sector operation, int and rem is standard math function of integer and reminder. The space vector diagram of a three-phase VSI is a hexagon, consisting of six sectors. SVPWM algorithm is to identify the triangle in which the tip of the reference vector is located. Each triangle can be treated as a vector of a two-level inverter. The ON-time can be calculated using small vector analogy ON-time equation of the two-level inverter. In each sector, triangle can be classified into two types. Type-1 triangle has its base side at the bottom. Type-2 triangle has its base side at the top. The triangle number Δj can be determined in terms of two integer variables I_1 and I_2 , which are dependent on the position of reference vector (V_α, V_β).

$$I_1 = \text{int} \left(V_\alpha + \frac{V_\beta}{\sqrt{3}} \right), \tag{19}$$

$$I_2 = \text{int} \left(\frac{V_\beta}{h} \right). \tag{20}$$

The Eq. (19) signifies part of the sector between the lines $y + \sqrt{3} = \sqrt{3}I_1$ and $y + \sqrt{3}x = \sqrt{3}(I_1 + 1)$. This forms one region and the Eq. (20) signifies part of the sector between the lines $y = hI_1$ and $y = h(I_1 + 1)$. This forms another region. The tip of reference vector is situated at the intersection of these two regions inclined at 120° and forms triangle or rhombus.

This rhombus is made of two triangles. Let $(V_{\alpha S}, V_{\beta S})$ are the co-ordinates of the reference vector with respect to the origin of the rhombus.

$$V_{\alpha S} = V_\alpha - I_1 + 0.5I_2, \tag{21}$$

$$V_{\beta S} = V_\beta - I_2h. \tag{22}$$

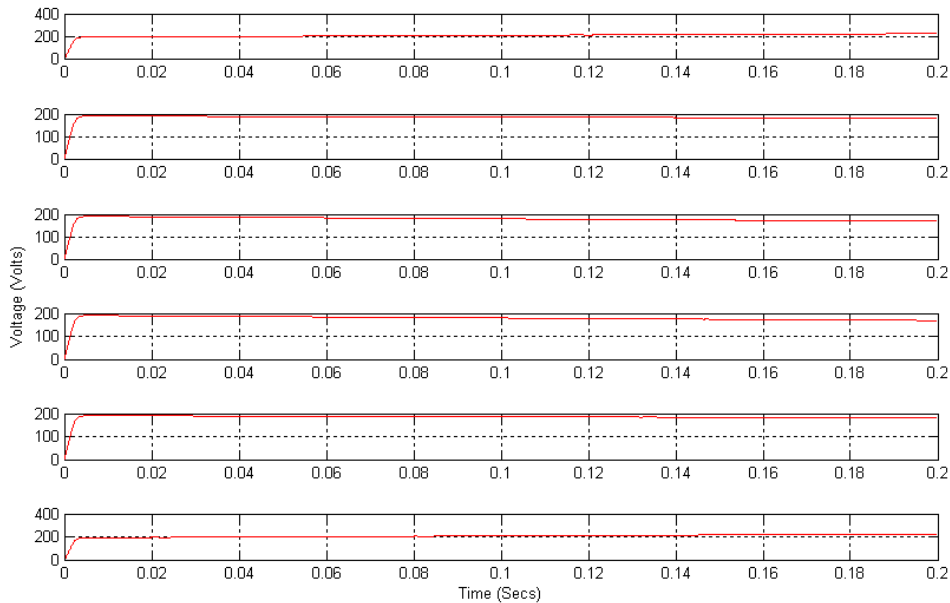


Fig. 4. DC link capacitor voltage for seven-level DCMLI

In Eq. (21) and Eq. (22), $(V_{\alpha S}/V_{\beta S})$ is the slope of the line between the origin of the rhombus and the reference vector and it is compared with slope of the diagonal of the rhombus which is $\sqrt{3}$. The slope comparison is done by evaluating inequality $(V_{\beta S} \leq \sqrt{3}V_{\alpha S})$ and to determine the small vector V^Z and the exact triangle number Δj . If the $(V_{\beta S} \leq \sqrt{3}V_{\alpha S})$, which indicates triangle of type-1 and these triangles are similar to sector-1 of two-level inverter. The triangle number Δj is obtained as

$$\Delta j = I_1^2 + 2I_2. \tag{23}$$

If $(V_{\beta S} > \sqrt{3}V_{\alpha S})$, which indicates the triangle of type-2 and these triangles are similar to sector 2 of two-level. The triangle number Δj is obtained as

$$\Delta j = I_1^2 + 2I_2 + 1. \tag{24}$$

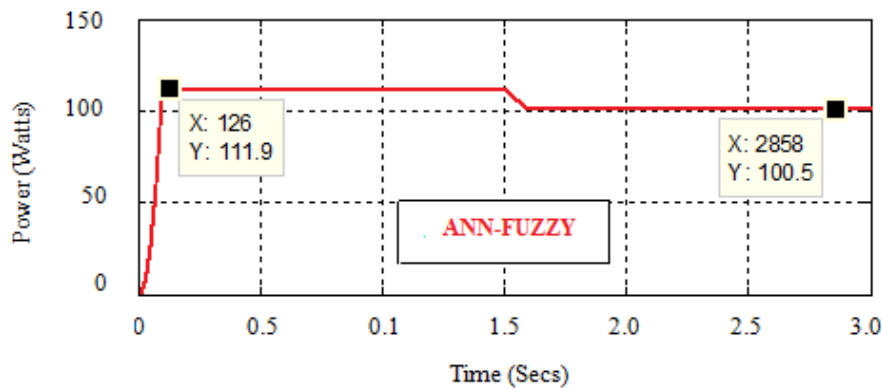


Fig. 5. Fuzzy MPPT tracking

In Eq. (23) and Eq. (24), Δ indicates the triangle and j is the triangle number and hence Δj is an integer and signifies j^{th} triangle in the sector. Using Eq. (23) and Eq. (24), to identify triangle in a sector and the on times are calculated using Eq. (14) to Eq. (16). The Δj is formulated to provide a simple way of arranging the triangle, leading to ease of identification and extension to any level and it greatly simplifies the PWM process as switching state can be easily mapped with respect to Δj .

6 Simulation result and discussion

Simulations are performed by using MATLAB/simulink for the proposed system. The SVPWM switching strategy is used in this paper. The SVPWM output is generated from this simulink module. The simulation was carried out for 0.2 seconds and this involves determining the position of reference vector according to fundamental frequency $f = 50$ Hz, sampling frequency $f_s = 10$ kHz and time. According to sector wherein the reference vector is, determine the switching sequence and to calculate the time for different switching states. The modulation index determines the shape of the output voltage of the inverter. Fig. 4 shows the results of multi DC link capacitor. It proves that the voltages are maintained constant.

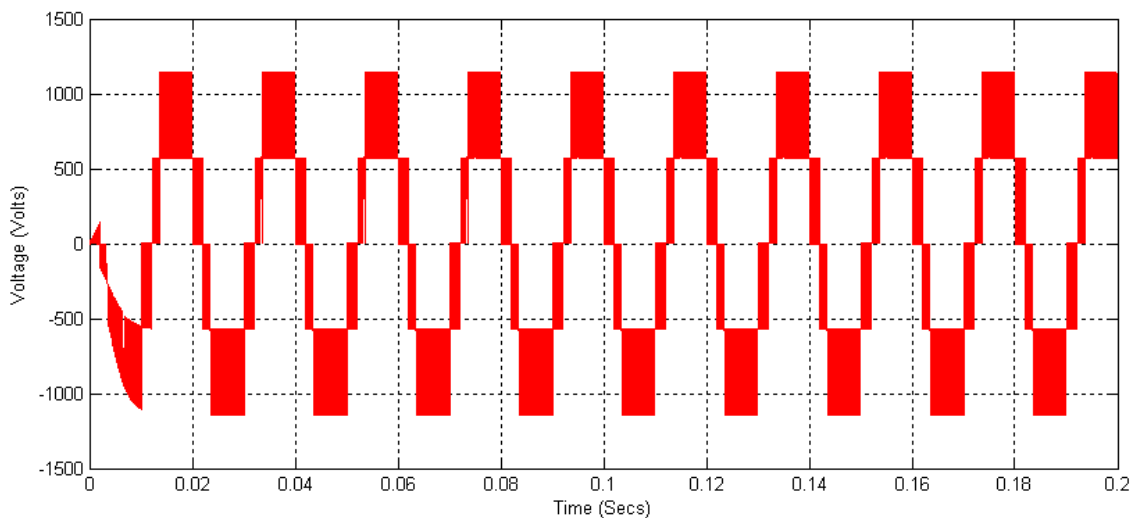


Fig. 6. Simulation result of a three-phase line-to-line (V_{ab}) voltage of DCMLI:three-level

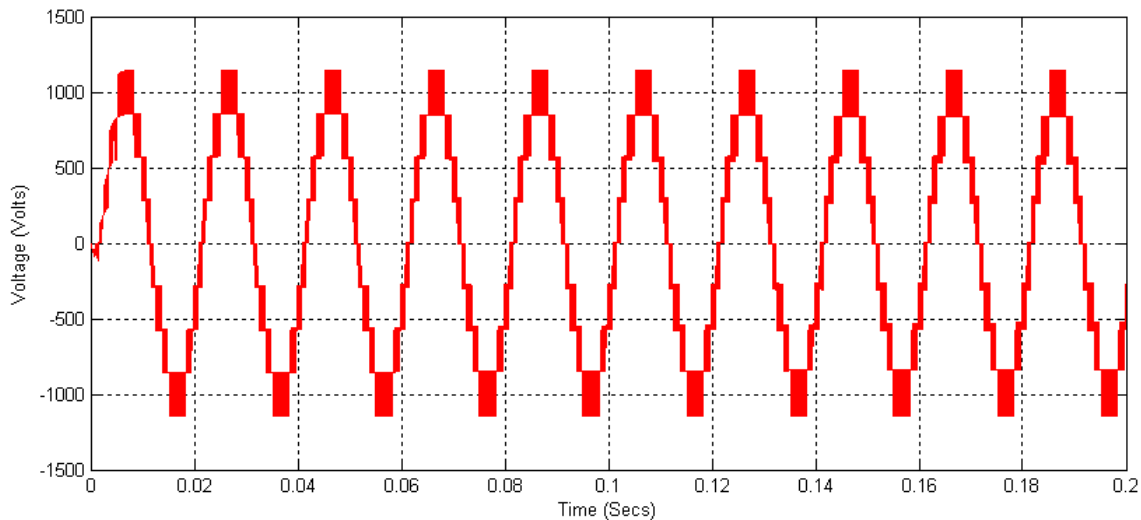


Fig. 7. Simulation result of a three-phase line-to-line (V_{ab}) voltage of DCMLI:five-level

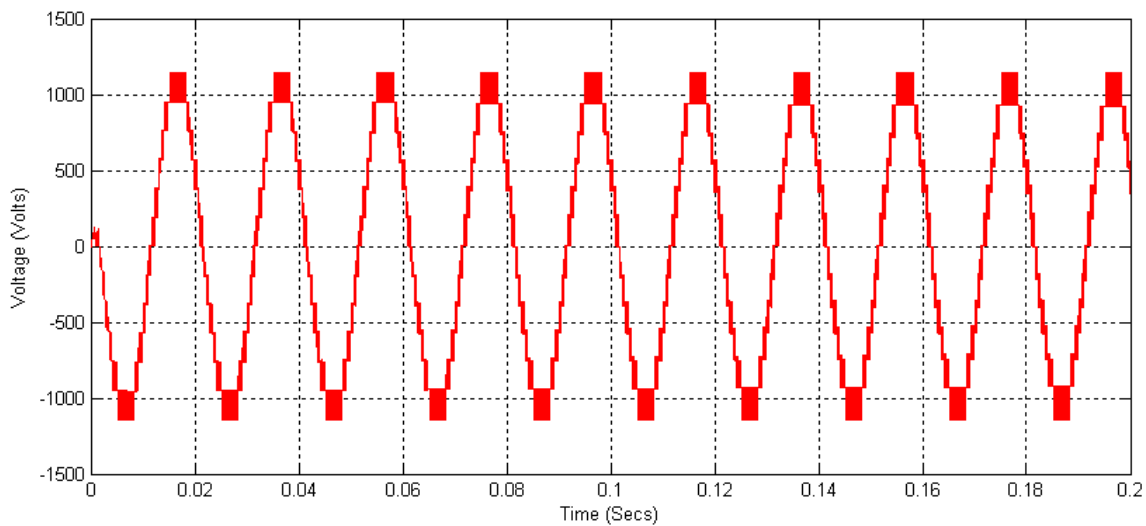


Fig. 8. Simulation result of a three-phase line-to-line (V_{ab}) voltage of DCMLI:seven-level

NFC controlled MPPT tracks the operating point quickly and accurately with and without change irradiance level. The simulation result of NFC MPPT tracking is shown in Fig. 5. The decoupling of the voltage loops V_d^* and V_q^* is good, since the V_q^* remains constant under variations which shows high dynamic performance of the controllers. The performance of the NFC with the PV DCMLI also shows that output of the PV follows its reference. The overall operation is governed by the control system where the controller samples the voltages of the inverter and then generates the SVPWM signals for driving the IGBTs. With the control scheme implementation, the inverter is able to maintain constant phase and line output voltage.

In the proposed system, the output line-to-line voltage of the three-phase three-level, five-level and seven-level DCMLI is shown in Fig.6, Fig. 7 and Fig. 8. This shows that the generated line-to-line voltage is much improved with the level of inverter. The performance of the NFC with the three-phase seven-level DCMLI also shows the output of PV follows its reference and there are no effects for the load variation. The simulation result of the output of the three-phase load connected three-level, five-level and seven-level DCMLI is shown in Fig.9, Fig. 10 and Fig. 11.

It can be seen that the output voltage and current waveforms are 50Hz sinusoidal, balance, and displaced to each other by 120° . It reveals a considerably good transient and steady-state performance of the inverter. The controller manages to precisely track the voltage reference, quickly achieve the steady-state values, and

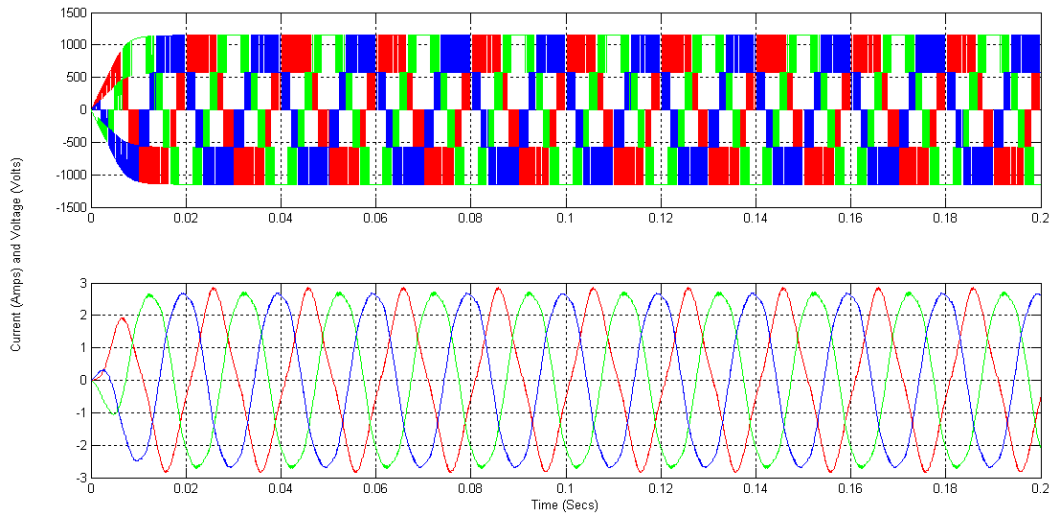


Fig. 9. Output of the three-phase load connected DCMLI:three-level

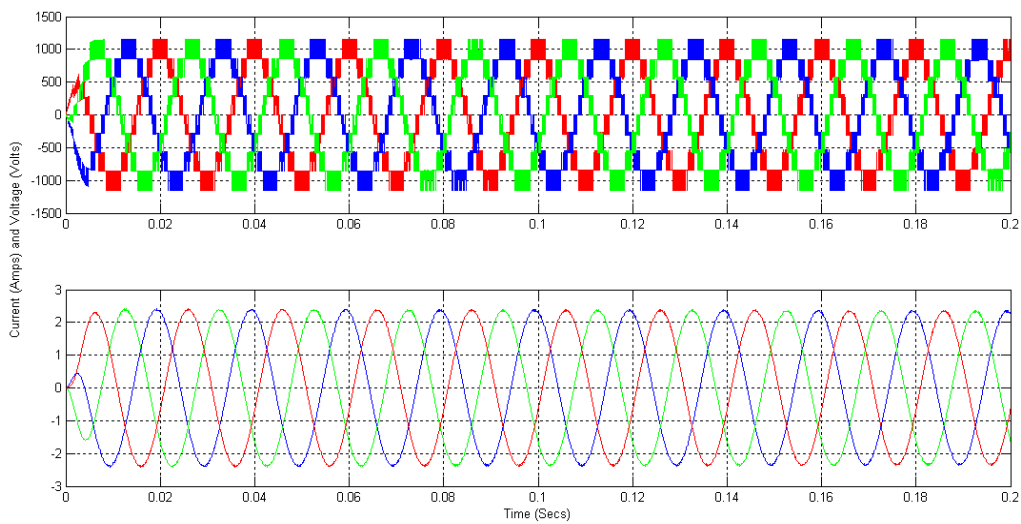


Fig. 10. Output of the three-phase load connected DCMLI:five-level

Table 2. Comparison between THD for proposed system with SVPWM

No of levels	Proposed SVPWM
3	0.30%
5	0.25%
7	0.19%

discriminates oscillation around the operating point. These results demonstrate the efficacy of the control strategy and algorithm employing the PI controller. Considering the phase relation of both load current and voltage waveform, they reveal in phase relationship, indicating a unity power factor feature which acquires high efficiency. This proves that the proposed scheme can reduce the THD which is an indispensable condition for PV system. According to the standard Std IEEE-929-2000, the THD of inverters output voltage waveforms must be less than 5%. The THD measurement of SVPWM three-level, five-level and seven-level DCMLI is shown in Fig.12, Fig. 13 and Fig. 14.

The THD measurement of SVPWM three-level and five-level are 0.30% and 0.25%. This show the THD, which is highly reduced as the level of inverter increases. From the results it is observed that the generated

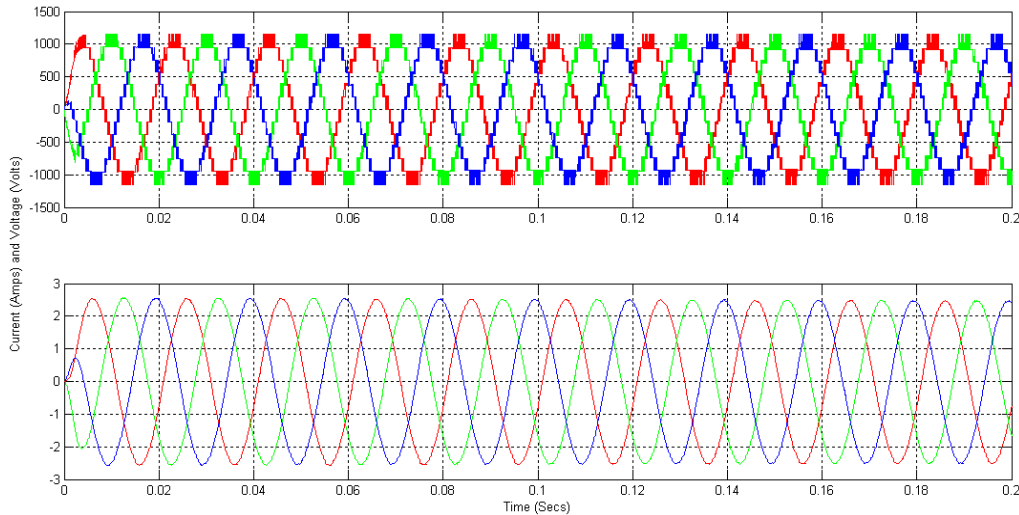


Fig. 11. Output of the three-phase load connected DCMLI:seven-level

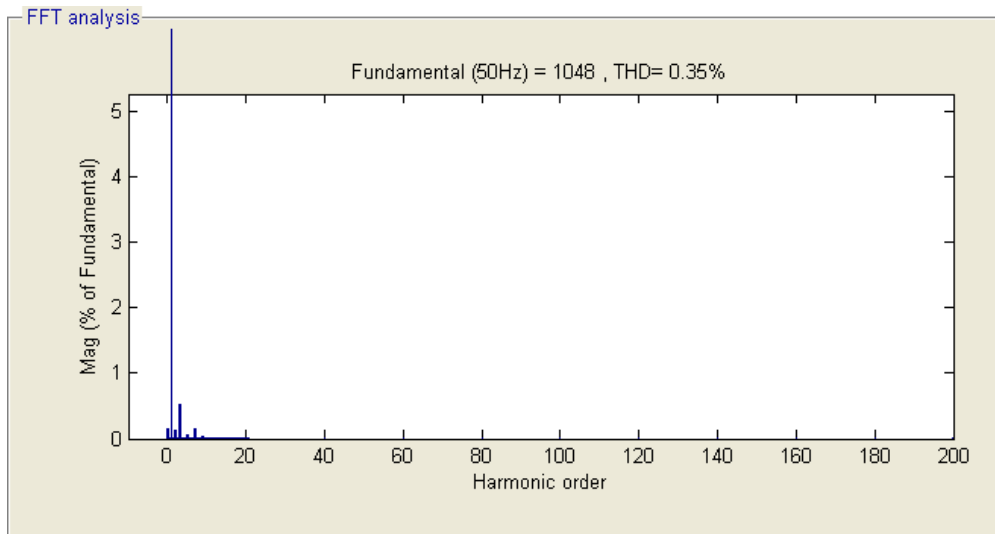


Fig. 12. THD measurement for DCMLI :three-level

voltage spectrum is very much increased with the level of inverter. The THD measurement of the proposed SVPWM seven-level inverter is 0.19%. The THD levels of proposed SVPWM three-phase three-level, five-level and seven-level inverters are compared in Tab.2. This proves that the proposed scheme can reduce the THD. The THD values of the proposed inverter are lower than that of the three-level and five-level DCMLI using SVPWM technique. The fundamental component of the output voltage is increased with the level of inverter. This shows that the generated line-to-line voltage is much improved with the level of inverter with SVPWM. The THD measurement of three-level and five-level DCMLI is 35.27% and 13.11%^[9]. The THD values are higher than the proposed inverter. This proves that the proposed scheme can reduce the THD which is necessary criterion for PV system.

7 Conclusion

This paper presents a three-phase seven-level DCMLI using SVPWM for photovoltaic systems. The configuration of the proposed system is designed and simulated using MATLAB/Simulink. This paper investigates the use of SVPWM of a three-phase DCMLI for photovoltaic systems to maximize DC link utilization, reduce

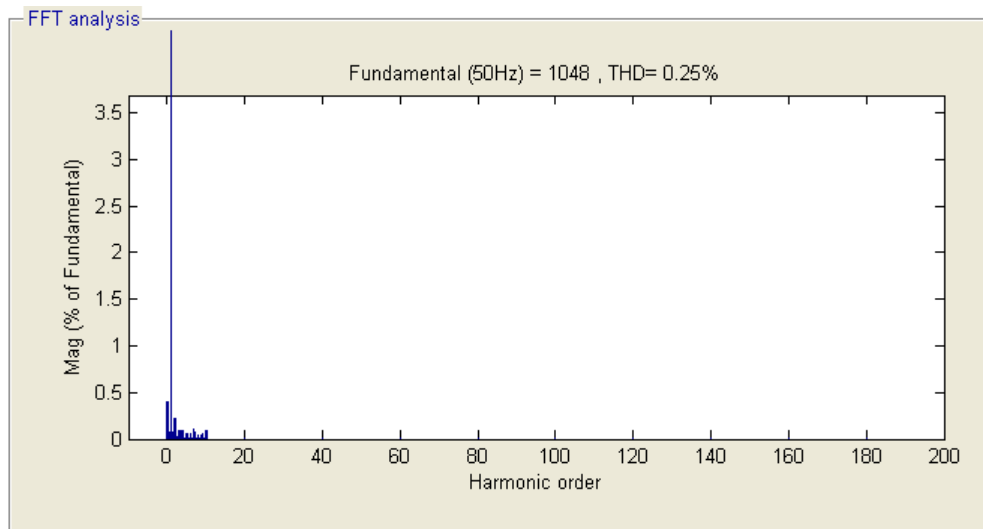


Fig. 13. THD measurement for DCMLI :five-level

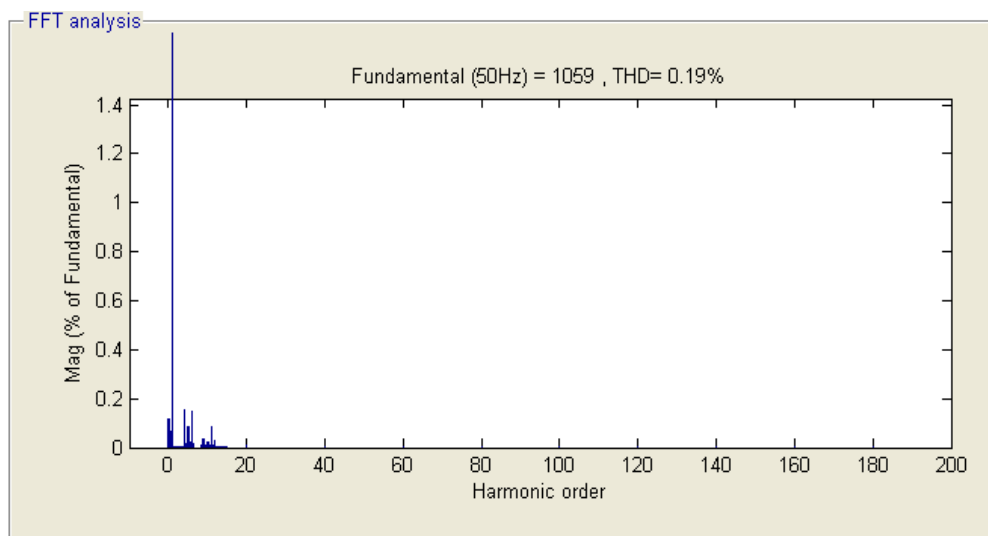


Fig. 14. THD measurement for DCMLI :seven-level

DC link capacitance and improve the quality of output voltage. The proposed system produces less d_v/d_t voltage stress imposed on the switching devices and the capacity to operate at a lower switching frequency. The proposed control scheme features has several advantages such as the generation of high quality currents, the capacity to operate at a lower switching frequency. NFC is more efficient than the conventional controller for nonlinear systems. The proposed fuzzy MPPT does not require an intermediate stage of DC-DC chopper control, as the optimum DC voltage is set by the inverter itself. The output of results reveals that the generated voltage spectrum is very much improved and also it minimize the overall THD of the output voltage of a MLI. The results obtained in this scheme, confirms that the use of DCMLI with SVPWM strategy are gained importance in high voltage, high power, and high performance applications such as PV generation system. The level of the inverter increases, the harmonic content of the output voltage waveform decreases. Thus, the output voltage quality increases with less THD for PV system.

References

- [1] U. Suresh Kumar, P. S. Manoharan. Economic analysis of hybrid power systems (PV/diesel) in different climatic zones of Tamil Nadu. *Energy Conversion and Management*, 2014, **80**: 469-476.
- [2] M. Villalva , J. Gazoli, et al. Comprehensive approach to modelling and simulation of photovoltaic arrays. *IEEE Transactions Power Electron*, 2009, **24**(5): 1198-1208.
- [3] J.Rodriguez , L. J.-Sheng, et al. Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Transactions Power Electron*, 2002, **49**(4): 724-738.
- [4] I. Colak , E. Kabalci,et al. Review of multilevel voltage source inverter topologies and control schemes. *Energy Convers. Manage* , 2011, **52**: 1114-1128.
- [5] F. Wu , K. Zhao ,et al. Simplified multilevel space vector pulse-width modulation scheme based on two-level space vector pulse-width modulation. *IET Power Electron* , 2012, **5**(5): 609-616.
- [6] E. Villanueva, P. Correa,et al. Control of a single-phase cascaded H-bridge multilevel inverter for grid connected photovoltaic systems. *IEEE Transactions Ind. Electron*, 2009, **56**(11): 4399-4406.
- [7] J. Selvaraj, N. Rahim. Multilevel inverter for grid-connected PV system employing digital PI controller. *IEEE Transactions Ind. Electron*, 2009, **56**(1): 149-158.
- [8] C. Cecati, F. Ciancetta, et al. A multilevel inverters for photovoltaic systems with fuzzy logic control. *IEEE Trans. Ind. Electron*, 2010, **57**(12): 4115-4125.
- [9] A. Ravi, P. Manoharan, et al. Modeling and simulation of three phase multilevel inverter for grid connected photovoltaic systems. *Solar Energy*, 2011, **85**: 2811-2818.
- [10] N. Yousefpoor, S. Fathi, et al. THD minimization applied directly on the line-to-line voltage of multilevel inverters. *IEEE Trans. Ind. Electron*, 2012, **59**(1):373-380.
- [11] Y. Liu, H. Hong, et al. Real-time algorithm for minimizing THD in multilevel inverters with unequal or varying voltage steps under staircase modulation. *IEEE Trans. Ind. Electron*, 2009, **56**(6):2249-2258.
- [12] M. Valan Rajkumar, P. S. Manoharan, et al. Simulation and an experimental investigation of SVPWM technique on a multilevel voltage source inverter for photovoltaic system. *Electrical Power and Energy Systems*, 2013, **52**: 116-131.
- [13] M. Valan Rajkumar, P. S. Manoharan. FPGA based multilevel inverters with SVPWM algorithm for photovoltaic system. *Solar Energy*, 2013, **87**: 229-245.