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Simulation and Experimental Based Four Switch Three Phase Inverter Fed Induction Motor Drive

Nalin Kant Mohanty[1*], Ranganath Muthu[2]

[1] EEE Department, Velammal Institute of Technology, Chennai, India
[2] EEE Department, SSN College of Engineering, Kalavakkam, Tamilnadu, India

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Abstract. A Simulation and experimental implementation of Four Switch Three phase inverter (FSTPI) fed Induction Motor drive is presented in this paper. In this proposed approach the simulation of the system is carried out using MATLAB/Simulink and experimental work is carried out using Spartan-3 processor and Xilinx software. In the experimental work, Xilinx software is used to generate the PWM pulses for FSTPI to drive the Induction Motor (IM). The proposed FSTPI fed IM drive is found acceptable considering its cost reduction and other advantageous features.

Keywords: FSTPI- four switch three phase inverter, FPGA-field programmable gate array, IM-induction motor, PWM-pulse width modulation

1 Introduction

AC induction motors, which contain a cage, are very popular in variable-speed drives. They are medium construction complexity, multiple fields in stator, cage on rotor, high reliability (no brush wear), medium efficiency at low speeds, high efficiency at high speed, low cost per horse power and easy to reverse the speed of motor. The induction motors are widespread used in industries over the years due to their relative cheapness, low maintenance, and high reliability. A large number of induction-motor control strategies have been investigated[4, 10, 14].

A standard three phase voltage source inverter utilizes six switches for three legs called Six Switch Three Phase Inverter (SSTPI), with a pair of complementary power switches per phase. A reduced switch count voltage source inverter consists of four switches i.e. Four Switch Three Phase Inverter (FSTPI) uses only two legs, with four switches. Several articles report on FSTPI structure[3, 5, 7, 8, 11, 12].

MATLAB is a high-level language and interactive environment for numerical computation, visualization, and programming. Simulink is a block diagram environment for multi domain simulation and Model-Based Design integrated with MATLAB. It supports system-level design, simulation, automatic code generation, and continuous test and verification of embedded systems. Simulink provides a graphical editor, customizable block libraries, and solvers for modeling and simulating dynamic systems[16]. The simulation of FSTPI fed IM is carried out in SIMULINK/MATLAB.

In this simulated work, three phase AC supply is converted into DC by using the three phase diode bridge rectifier. The DC power is converted into AC power through the FSTPI to drive the three phase induction motor. This drive system is designed in using in built blocks of MATLAB/Simulink. The inbuilt blocks are arranged according to the needs of the user and the outputs are shown in scope in SIMULINK/MATLAB.

The hardware implementation work is carried out using FPGA and Spartan-3 processor. Field Programmable Gate Array (FPGA) is a type of logic chip that can be programmed. An FPGA is similar to a

* Corresponding author. *E-mail address*: nkmtech@gmail.com.

PLD, but whereas PLDs are generally limited to hundreds of gates, FPGA supports thousands of gates. They are especially popular for prototyping integrated circuit designs. Once the design is set, hardwired chips are produced for faster performance. The inherent parallelism of the logic resources on an FPGA allows for considerable computational through put even at a low MHz clock rates. The flexibility of the FPGA allows for even higher performance by trading off precision and range in the number format for an increased number of parallel arithmetic units. This has driven a new type of processing called reconfigurable computing, where time intensive tasks are offloaded from software to FPGA[13]. Another important advantage of VHDL is that it is technology independent. The same algorithm can be synthesized into any FPGA and even has a direct path to an ASIC, opening interesting possibility in industrial applications in terms of performance and cost. However, the major disadvantage of an FPGA-based system for hardware implementation is the limited capacity of available cells. The FPGA-based applications of various motor drives can be found in [6, 9, 15].

The Spartan-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to 5,000,000 system gates. The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. These Spartan-3 FPGA enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic[2].

In hardware implementation, XILINX FPGA is used to generate PWM pulses for FSTPI and the motor is fed from a four switch three phase PWM inverter instead of a conventional six switch three phase inverter. VHDL (Very high speed IC description language) program is developed and simulated in XILINX software and implemented on a Spartan-3 Processor. Simulation and experimental results illustrate the use of the FSTPI to drive three phase induction motor.

2 Proposed topology

The block diagram of proposed simulation and FPGA based FSTPI fed IM drive is shown in Fig. 1. The diode bridge rectifier converts three phase AC to DC. The FSTPI is used to convert DC to three phases AC, which is used to drive the induction motor. The FPGA is used to generate PWM pulse to control the FSTPI. The FPGA processor output pulses are fed to the inverter through driver circuit to drive the Induction Motor through FSTPI.

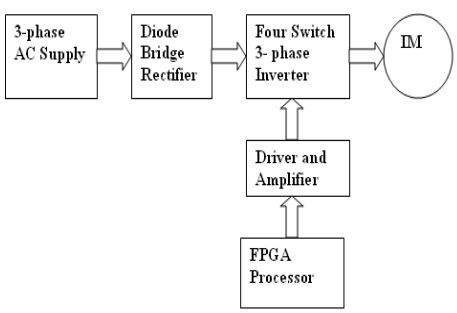


Fig. 1. Block diagram of FPGA based FSTPI

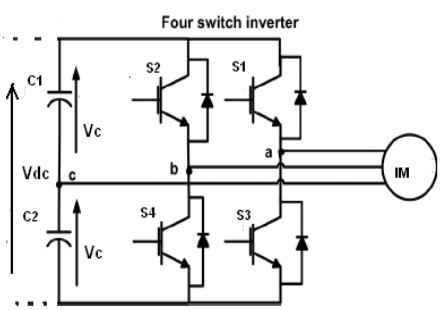


Fig. 2. FSTPI with induction motor

3 Principle of operation of FSTPI

The power circuit of the FSTPI fed IM drive is shown in Fig. 2. The FSTPI has 4 switches, namely S_1, S_2, S_3 and S_4 and a split capacitor. The switches are controlled in order to generate an AC output from the

DC input. The two phases 'a' and 'b' are connected through two legs of the inverter, while the third phase 'c' is connected to the center point of the DC link capacitors, C_1 and C_2. The capacitance value of C_1 and C_2 are equal. It is assumed that the 4-power switches are denoted by the binary variables S_1 to S_4. The binary '1' corresponds to an ON state and the binary '0' corresponds to an OFF state. The states of the upper (S_1, S_2) and lower (S_3, S_4) switches of a leg are complementary that is $S_3 = 1 - S_1$ and $S_4 = 1 - S_2$. Considering a 3-phase Y-connected Induction Motor, the terminal voltages V_{as}, V_{bs} and V_{cs} can be expressed as the function of the states of the upper switches as follows[9]:

$$V_{as} = \frac{V_c}{3}(4S_1 - 2S_2 - 1), \tag{1}$$

$$V_{bs} = \frac{V_c}{3}(-2S_1 + 4S_2 - 1), \tag{2}$$

$$V_{cs} = \frac{V_c}{3}(-2S_1 - 2S_2 + 2), \tag{3}$$

where V_{as}, V_{bs}, V_{cs} are the inverter output phase voltages. 'V_c' is the voltage across the DC link capacitors. 'V_{dc}' is the voltage across the capacitor C_1 and C_2 ($V_{dc} = V_c/2$). S_1, S_2 are taken as the switching functions for the 2-switches. In matrix form the above equations can be written as:

$$\begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix} = \frac{V_c}{3} \begin{pmatrix} 4 & -2 \\ -2 & 4 \\ -2 & -2 \end{pmatrix} \begin{bmatrix} S_1 \\ S_2 \end{bmatrix} + \frac{V_c}{3} \begin{bmatrix} -1 \\ -1 \\ 2 \end{bmatrix}. \tag{4}$$

Tab. 1 shows the different modes of operation and the corresponding output phase voltage vector of the FSTPI.

4 Simulation of FSTPI fed IM drive

The simulation model has been developed to test the proposed FSTPI fed IM drive by using MATLAB/Simulink. The simulations were performed for a FSTPI fed IM drive at no load and load conditions. The drive system consists of a three phase diode bridge rectifier, a split capacitor, four switch three phase inverter, 3-phase squirrel cage Induction Motor. The parameter of Induction motor used in this simulation work is given in the Tab. 2.

Table 1. Switching states and output phase voltages of FSTPI

Switching states		Output voltage		
S_1	S_2	V_{as}	V_{bs}	V_{cs}
0	0	$-\frac{V_c}{3}$	$-\frac{V_c}{3}$	$\frac{2V_c}{3}$
0	1	$-V_c$	V_c	0
1	0	V_c	$-V_c$	0
1	1	$\frac{V_c}{3}$	$\frac{V_c}{3}$	$-\frac{2V_c}{3}$

Table 2. Switching states and output phase voltages of FSTPI

Motor rating	0.5 Hp, 380V, 4-pole, 50 Hz
Stator resistance	11.1Ω
Stator inductance	18.8mH
Rotor resistance	12.3Ω
Rotor inductance	26.7mH
Magnetizing inductance	467mH
Inertia kg m^2	0.01
Friction coefficient Kdf	0.02

Fig. 3 shows the PWM block and FSTPI fed IM. The PWM block provides the required PWM pulses for the 4-switches of FSTPI. Fig. 4 shows the complete simulation circuit diagram of the system. The 3-phase output currents of FSTPI are shown in Fig. 5. A balanced 3-phase output current is obtained at the output of FSTPI.

The speed and torque curve of Induction motor is shown in Fig. 6 (a) and in Fig. 6 (b) without and with load conditions. With no load condition the speed of motor increased linearly and reached at near rated

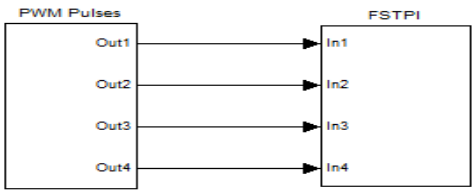


Fig. 3. Block diagram of PWM pulses with FSTPI in Simulink

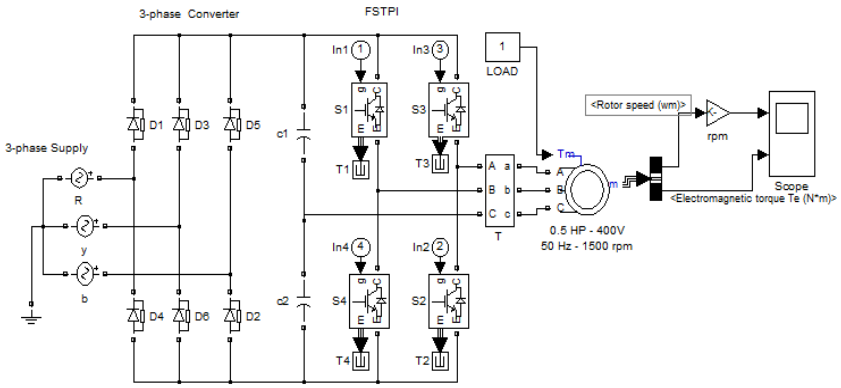


Fig. 4. Complete simulation circuit diagram of FSTPI fed IM drive system

speed (1500 rpm) at required speed in steady state at 2 second. At starting the torque increases and reaches at minimum value when the speed reaches at rated value. In Fig. 4, a 1 KN load is applied at the motor terminal. It is observed that the speed of IM increased linearly from zero and reached at 1350 rpm at 3 second.

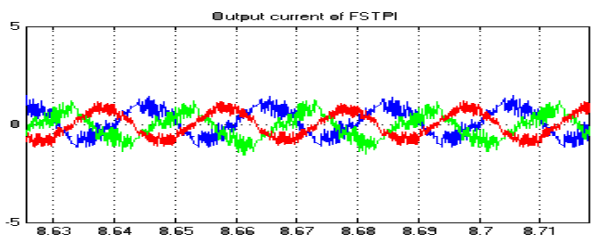
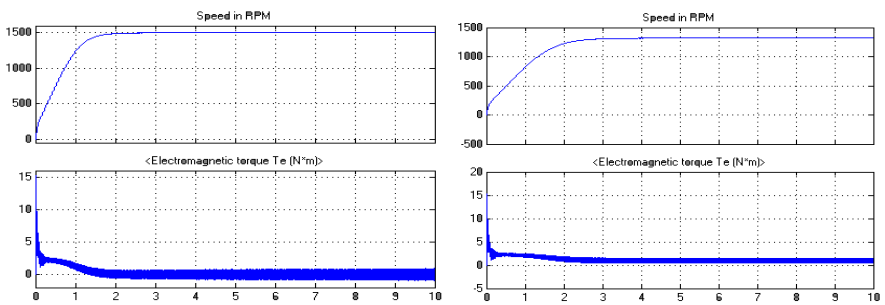


Fig. 5. Three phase current of FSTPI



(a) (b)

Fig. 6. Rotor speed in rpm and torque in N-m vs time in sec. (a) without load (b) with load

5 Experimental implementation

To establish the feasibility of system, the experimental implementation is carried out using Xilinx software with SPARTAN-3 processor. This is equipped with appropriate plug-in boards for power switch control. The multi meter and digital storage oscilloscope is used to measure the output current and voltage of FSTPI. A complete hardware setup is described in the Tab. 3.

Table 3. Hardware component details

Components	Ratings
Capacitor	1000μf, 250V
Inverter	MOSFET (IRF 460)- 4Nos
Induction Motor	0.5 hp ,3-phase, 50Hz,400V
Processor	SPARTAN-3, model XC3S200
Rectifier	110+Nos,5A Diode Bridge Rectifier
Driver Circuit Board	—

The complete set up (FPGA processor board, Driver Circuit, FSTPI, and 3-phase IM) is shown in Fig. 7. The output pulses waveforms of switch S_1, S_2, S_3, and S_4 are obtained from the driver circuit are taken by the Digital Storage Oscilloscope. The pulses of switch S_1 is shown in Fig. 8.

The output current waveform of phase-A is shown in Fig. 9. It is found that the simulation and experimental results are almost similar. The simulation and experiment work of FSTPI fed Induction motor drive carried out successfully.

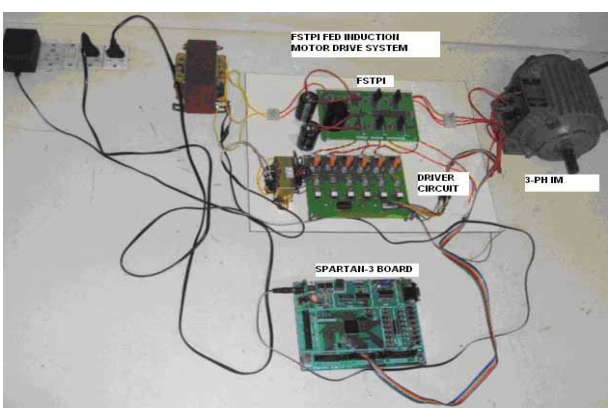


Fig. 7. A complete hardware set up of FPGA based FSTPI drive

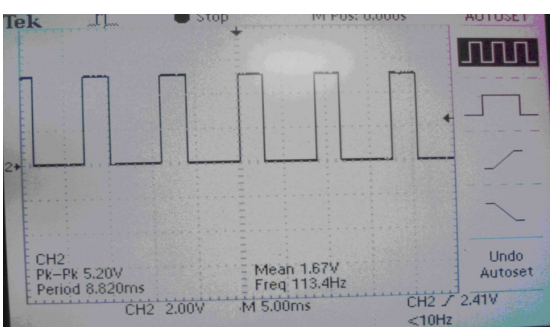


Fig. 8. Pulses of switches S_1

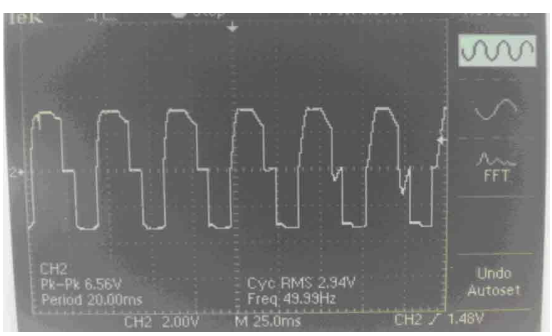


Fig. 9. Output current of FSTPI of phase A

6 Conclusion

The simulation and hardware implementation of FSTPI fed IM drive is carried out successfully. In the simulation work the FSTPI fed induction motor is simulated with load and without load conditions. The results are obtained such as the speed and torque characteristics of induction motor are found satisfactory. To test the feasibility of FSTPI fed IM drive, hardware implementation is carried out by using Xilinx software and Spartan-3 processor. VHDL (Very high speed description language) program is developed and simulated in XILINX software and loaded to FPGA Spartan processor, to generate PWM pulses for driving the IM. In the hardware work, the induction motor has run successfully.

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