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3D Simulation-Based Research on the Effect of Interconnect Structures on Circuit Reliability

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Abstract. Electromigration (EM) of the interconnects is a key factor in determining the reliability of an integrated circuit, especially for the present-day IC with shrinking interconnect dimension. The simulation of the EM reliability of the interconnects is usually performed using the line-via structure at the EM test temperature (e.g. 300 oC).However, such simulation using the line-via structure may not give the same void nucleation location as in the real circuit structure, especially at the circuit operation temperature (e.g. 90 oC). This change in failure site can cause mis-interpretation of the EM weak spot location when the line-via structure is used for data extrapolation in predicting the EM reliability of the entire circuit. This drives the need for the reliability simulation using a complete 3D circuit model. In this paper, we build several 3D models of a simple circuit with different interconnect structures and examine the effect of the layout structural changes, such as the via and contact positions and their numbers, the inter-transistor distance, the metal structure and layer number, on the circuit EM reliability. 3D circuit model. In this paper, we build several 3D models of a simple circuit with different interconnect structures and examine the effect of the layout structural changes, such as the via and contact positions and their numbers, the inter-transistor distance, the metal structure and layer number, on the circuit EM reliability. A 585.40% improvement in the EM lifetime can be obtained by using Metal 1 as the output line instead of the metal/via stacks, while a 136.97% reduction in the EM lifetime is observed when the number of contacts of the transistor reduces from 6 to 3.The simulation results are consistent with the experimental results in the literature and thus validate the capability of performing the EM lifetime comparison of different interconnect structures using the 3D circuit model.

Keywords: 3D modelling, finite element analysis, electromingration, interconnect reliability

1 Introduction

As the ULSI technology progresses, the increasing complexity of the ICs makes the reliability simulation before fabrication necessary in order to avoid re-design and re-fabrication. Among the various reliability degradation mechanism, electromigration (EM) is found to be the most dominating failure mechanism for the interconnect reliability[35], and it is gaining a lot of attentions by the researches.

The interconnects' EM reliability of an integrated circuit were usually predicted by the 2-dimensional (2D) EM simulators[3, 12, 18, 21, 29, 34, 40]. The traditional 2D circuit simulators assumed a constant temperature across the surface of the chip[12, 18, 21, 34]. This assumption is no longer valid in high density ICs with multiple metal layers, as the temperature difference at different portions of the chip may vary by 50ºC or more and that between the top-most and the lowest layer of the metallization can be larger than 45ºC[2]. Temperature is a key factor in determining the degradation rate of the interconnects and its surrounding materials[1]. Therefore, the temperature effects cannot be ignored and the later EM simulators do take these effects into consideration[3, 29, 40]. However, with the development of the new technologies like SIC (stacked-integrated-

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circuit), SOC (system-on-chip) and SiP (system-in-package), the vertical stacking of the circuits and the overlapping of the metal layers make it difficult for the application of the simulators at 2D level. Moreover, the 2D circuit simulators treated current density as the main consideration for EM and ignored the thermo-mechanical stress effects. The work by Li et al. [19] showed that the thermo-mechanical stress was the dominant factor in determining the interconnect EM reliability when the line width is below 200 nm and should not be ignored. With the scaling of the interconnect dimension and the increasing in the number of metal layers, it becomes increasingly difficult to simply use 2D simulations for an efficient and effective EM awareness design. Therefore, the 3D model with the consideration of all the factors for EM is needed when accessing the EM reliability of the circuit.

To cater for the temperature and thermo-mechanical stress effects, as well as other factors that are important to EM, the physics based EM models had been developed and improved from 1D[9, 25, 32] to 2D[36], and finally to 3D[10, 28, 30, 31]. The physics based 3D EM models were able to include all the factors that affect the EM reliability, and they considered both the structural and the material effects for both the interconnect line itself and the surrounding materials. Therefore the simulation results are much more accurate as compared with the 1D or 2D models and simulators. For a comprehensive review on the EM reliability study and the physics based EM models, please refer to the work by Tan et al. [38, 39].

However, the complexity of the 3D models limited its application at the circuit level. The 3D EM modelling were usually performed only at the localized region of an interconnect tree, e.g., on a simple metal line or at the line-via region. These structures are only part of the real circuit structures and the results obtained from these partial-circuit structures can only represent the reliability of the respective localized region. The impact of excluding the rest of the circuit structures to the overall EM reliability of the circuit has not been investigated. In our previous study in [17], it was found that although the line-via structure showed the same maximum atomic flux divergence (AFD) location (i.e. the void nucleation location) as in the circuit structure under the EM test condition of 300ºC, the maximum AFD locations of the two structures are different under the circuit operation condition of 90ºC. The comparison the maximum AFD locations of the two structures under the two test conditions is shown in Figs. 1 and 2 and summarized in Tab. 1. In Fig. 1, the maximum AFD locations are found at the Metal 1/Via 12 interface for both structures[17]. In Fig. 2, the maximum AFD locations are different for the two structures[17].

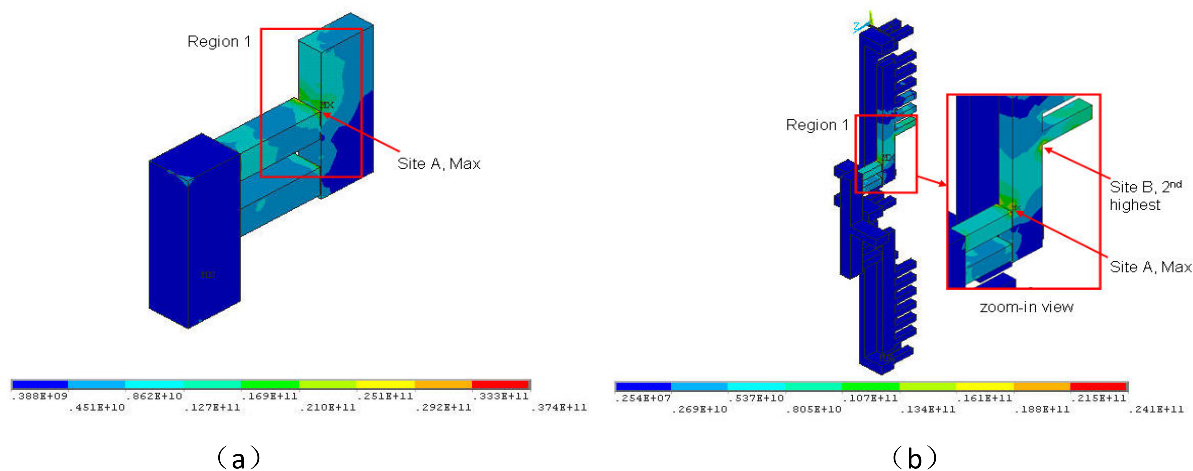

Fig. 1. The total AFD distributions of (a) the line-via structure and (b) the circuit structure at 300 oC (unit: atoms/μm^3 · s)

In addition, the surrounding materials and the architecture of the circuit have an impact on the distributions of the current density, temperature, and thermo-mechanical stress of the interconnects, and these in turn affect the distributions of the atomic flux divergences and the lifetime of the circuit. For example, the use of the low-k dielectrics could result in a higher circuit temperature due to their poorer thermal conductivities as compared to the traditional SiO2 dielectric[15]. Furthermore, due to the larger thermal expansion coefficients

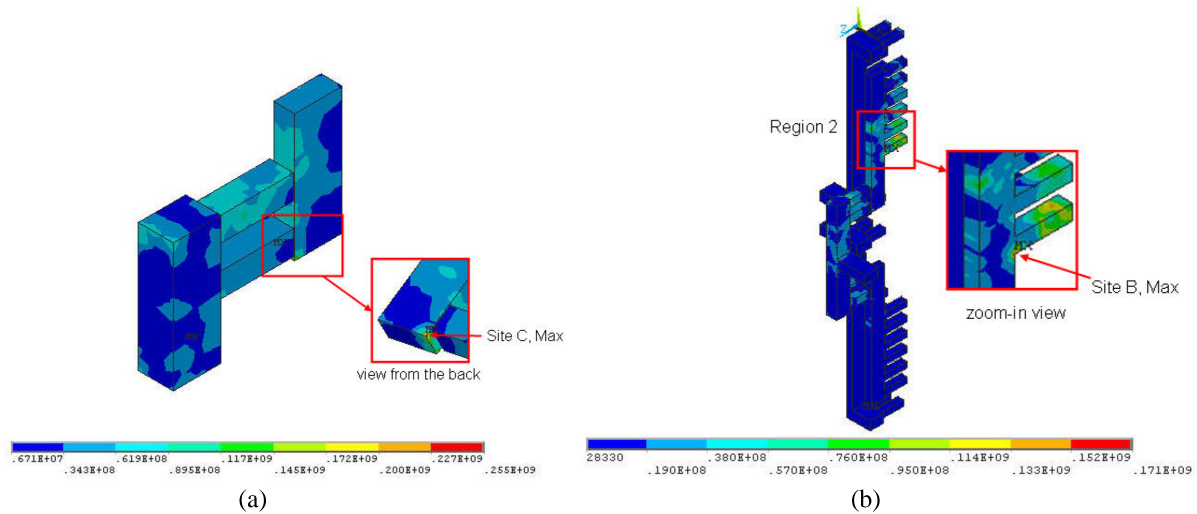

Fig. 2. The total AFD distributions of (a) the line-via structure and (b) the circuit structure at 90 oC (unit: atoms/μm^3 · s)

Table 1. The maximum AFD locations of the line-via structure and the circuit structure under different conditions

Structure	Maximum AFD location	
	EM test condition	Circuit operation condition
Line-via structure	Metal 1/Via 12 interface	corner of Metal 1
Circuit structure	Metal 1/Via 12 interface	contact/Metal 1 interface

and the smaller elastic modules of the low-k materials, an increase in the thermo-mechanical stress gradient or even a change of tensile stress to become compressive stress was observed in the Cu/low-k structure[16]. A decrease in the substrate dimension from 1000 μm 1000 μm (length width) to 20 μm 20 μm could cause nearly 30% increase in the final circuit temperature[15].

Therefore, simple line-via structure is not a suitable choice if we want to study the EM reliability of the entire circuit under the circuit operation condition.

The 3D simulations of the effects of the interconnect structures on the EM reliability in the literature[4, 8, 13, 14, 20, 22, 41, 43] were all performed at the line-via structure level (i.e. the partial-circuit level). As stated previously, the EM modelling at the “localized” regions may not represent the EM reliability of the entire circuit, and the circuit EM reliability is affected by the properties and the dimension of the surrounding materials. To study the effect of interconnect structures on the circuit EM reliability, the entire chip structure should be considered. In this paper, as an extension to our previous work in [17], a series of 3D models with different interconnect structures are built at the circuit level. The entire chip structure, including the interconnects, the circuit components, the substrate, the dielectric, as well as the packaging are included in the model, so as to accurately model the EM reliability of the entire circuit. The structures that can most effectively enhance the circuit reliability are investigated through the finite element analysis using ANSYS.

In the next section, the simulation setup for the 3D circuit model will be presented. The output stage of a simple class-AB amplifier is used as an example. The formulation of the problem based on the AFD approach will be presented in Section 3 and the discussion on the results obtained will be given in Section 4. This paper ends with a conclusion and a plan for the future work in Section 5.

2 Simulation setup

Class-AB amplifier is a common building block of an analog amplifier circuit. The output stage of the class-AB amplifier is vulnerable to EM due to the large current flow. To reduce the complexity of the work, only the output stage is used as an example. The circuit schematic is shown in Fig. 3. The short circuit

protections (not shown in the schematic for clarity) are not included in the model construction as they do not affect the current density, temperature, and thermo-mechanical stress distributions of the model.

To minimize the size of the 3D model, the sizes of the p-channel MOSFET (PMOS) and the n-channel MOSFET (NMOS) are kept small ($W = 3\mu m$, $L = 0.18\mu m$). The supply voltage from Vdd is 3.30 V and the input voltage Vin is 0.70 V. The circuit operates under small signal excitation with a frequency of 100 MHz and drives a resistive load of 1 kΩ[5]. Other loadings and operating frequencies can be used depending on the application of the circuits. The source and the drain currents and voltages of the transistors are extracted from Cadence and used as the inputs of the 3D model in ANSYS.

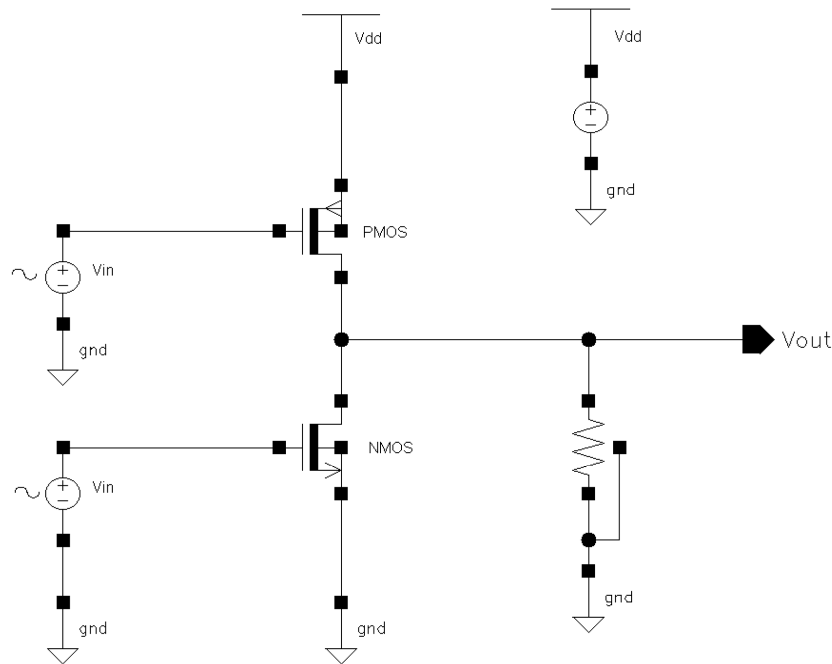

Fig. 3. The schematic of the output stage of a class-AB amplifier

In Fig. 4, the side views of the circuit models with different interconnect structures. An example of the 3D class-AB amplifier circuit model constructed from the 2D layout is shown in Fig. 4(a). The detailed steps of the 3D model construction can be found in our previous work [15, 37]. In order to study the effect of the interconnect structures on the circuit reliability, several 3D models with the following changes as shown in Categories (I) to (V) are constructed.

(I) Change in the position of the vias: The vias are moved from the extreme end of Metal 1 (Fig. 4(a)) to the region closer to the contacts (Fig. 4(b)), and directly above the contacts (Fig. 4(c)).

(II) Change in the inter-transistor distance: The inter-transistor distance (i.e. the distance between the diffusion regions of the PMOS and NMOS) is varied from 2 μm (i.e. minimum distance, Fig. 4(d)) to 5 m (Fig. 4(e)) and then to 8 m (Fig. 4(f)).

(III) Change in the number and the position of the contacts: The number of contacts at the source and drain regions is reduced from 6 in Fig. 4(d) to 3, with the contact position directly below the vias (Fig. 4(g)) and at the other end of Metal 1 (Fig. 4(h)).

(IV) Change in the metal structure at the output line: Metal 1 is used as the output line instead of Metal 2 (Fig. 4(i)).

(V) Change in the number and the position of the metal layers: In the real circuit, the output line of the transistor may connect to the next stage directly via Metal 2 or Metal 1 (e.g. to another transistor, like in Figs. 4(a) $\sim$ 4(i)), or via Metal 1 to Metal 6 (e.g. to a capacitor or inductor, or to the output pad). The connection may be directly above the transistor (Fig. 4(j)), or at a distance away from the transistor (Fig. 4(k)). For easy comparison purpose, similar structures are used in Figs. 4(j) and 4(k).

The circuit performances of the above structures remain unchanged as verified by Cadence. The simulation is carried out under the circuit operation condition of 90ºC. The size of the Si substrate of the model is 1000 μm 1000 μm 300 μm (length $\times$ width $\times$ thickness, roughly the size of a die) which is much larger than the circuit in the center, so as to avoid any temperature effect due to the substrate dimension as explained previously. The circuit model is enclosed by the encapsulation and attached to the metal plate via the die attach to represent the realistic chip condition[37]. The base of the model (i.e. the metal plate base) is treated as the heat sink and is not free to move. The boundary conditions of the electro-thermo-structural simulation are shown in Fig. 5.

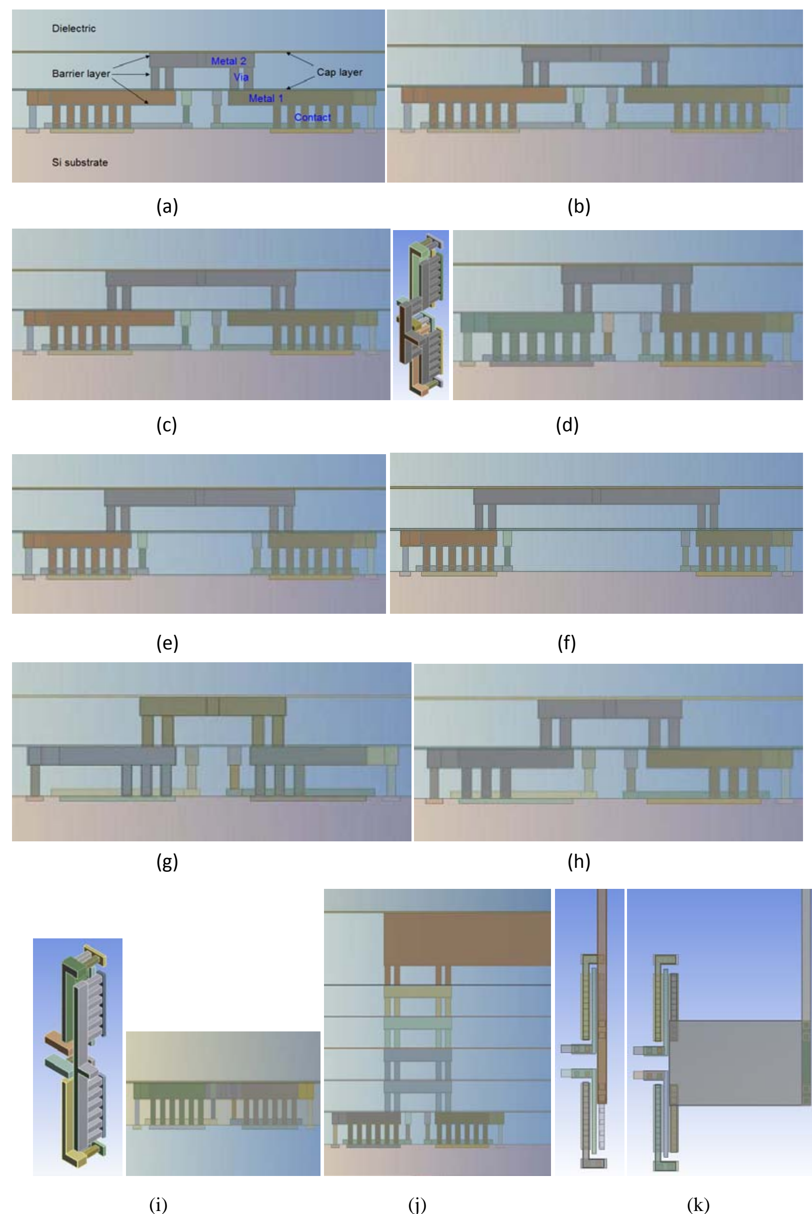

Fig. 4. (a) The vias positioned far away from the contact region (b) the vias positioned nearer to the contact region (c) the vias positioned directly above the contact region (d) an inter-transistor distance of 2 μm (the isometric and the side view) (e) an inter-transistor distance of 5 μm (f) an inter-transistor distance of 8 μm (g) 3 contacts positioned directly below the vias (h) 3 contacts positioned at the other end of Metal 1 (i) Metal 1 used as the output line (the isometric and the side view) (j) 6 metal layers positioned directly above the transistor (the side and the plain view) and (k) 6 metal layers positioned at a distance of 5 μm away from the transistor (the plain view)

The skin depth at the frequency of 100 MHz is larger than the thicknesses of Metal 1, Metal 2, Via 12 and the contacts, thus skin effect is ignored in this study. Due to the scale of the problem and as we are focusing on the initial void nucleation location of the interconnects, the microstructure effect and the stress relaxation effect of the interconnects is assumed to be negligible. Quadratic tetrahedral element type SOLID 98 is used in the ANSYS simulation. The current loads are applied at the contact/diffusion region interface, and the voltage loads are applied at the top metal (Metal 2 for Structures (a) to (i) and Metal 6 for Structures (j) and (k)). The material properties used in the model and the variation of thermal conductivity with temperature for some of the materials are listed in Tabs. 2 and 3 respectively.

Table 2. The material properties used in the model[7, 23, 42]

Materials	Properties						
	Young's Modulus (MPa)	Poisson's Ratio	Density (kg/m^3)	Thermal Expansion (1/ºC)	Thermal Conductivity (W/mºC)	Specific Heat (J/kgºC)	Resistivity (Ohmm)
Cu	1.10×10^5	0.34	8300	1.80×10^{-5}	403	385	1.72×10^{-8}
Si Substrate	1.30×10^5	0.28	2330	2.60×10^{-6}	149	700	1.00×10^{17}
As-doped Si							9.90×10^{-3}
B-doped Si							2.81×10^{-2}
Heavily doped Si							1.00×10^{-5}
SiO2	7.14×10^4	0.16	2200	6.80×10^{-7}	1.38	1000	1.00×10^{17}
SiN	2.20×10^5	0.27	3100	3.20×10^{-6}	30	700	1.00×10^{13}
Ta	1.86×10^5	0.34	16690	6.30×10^{-7}	57.50	140	1.31×10^{-7}
Polyimide	3100	0.33	1430	5.00×10^{-5}	0.18	1100	1.00×10^{15}
96% Alumina	276	0.25	3965	7.10×10^{-6}	20.90	779	1.00×10^{13}

Table 3. The temperature dependency of thermal conductivity for some materials[11].

Materials	Thermal Conductivity (W/moC)					
	0 ºC	27 ºC	127 ºC	227 ºC	327 ºC	427 ºC
Cu	403	395	390	380	370	365
Si Substrate	149	148	99	76	62	51
SiO_2	1.38	1.38	1.51	1.61	1.75	1.92

3 The atomic flux divergence approach

Atomic flux divergence (AFD) is the main cause for metallization EM degradation[39]. Finite element analysis using the AFD approach is a common practice in the modelling and simulation for the study of EM and the EM lifetime shows an inverse relationship with the AFD[6]. Void is found to nucleate at the location with the highest positive AFD and grows irreversibly[39]. This irreversible growth causes the void nucleation location to be the EM weak spot of the interconnects and a potential location of failure. The experimental observation in [26] showed that the void is found at the location with the maximum AFD, which proves the accuracy of the AFD approach.

The AFD approach is used in this study to model the EM reliability of the interconnects. There are three main factors contributing to the AFD, namely the electrical, thermal, and thermo-mechanical stress effects. These three factors result in three driving forces, namely the electron wind force, the temperature gradient induced driving force, and the thermo-mechanical stress gradient induced driving force. The atomic fluxes due to the three driving forces are calculated using Eq. (1) $\sim$ (3) respectively[10],

$$\vec{J}_{EWF} = \frac{N}{k_B T} eZ^* j\rho D_0 \exp(-\frac{E_A}{k_B T}), \tag{1}$$

$$\vec{J_T} = -\frac{NQ^* D_0}{k_B T^2} \exp(-\frac{E_A}{k_B T}) gradT, \tag{2}$$

$$\vec{J_S} = \frac{N\Omega D_0}{k_B T} \exp(-\frac{E_A}{k_B T}) grad\sigma_H, \tag{3}$$

where J_{EWF}, J_T and J_S are the atomic fluxes due to electron wind force, temperature gradient induced driving force and thermo-mechanical stress gradient induced driving force respectively, N is the atomic density, k_B is the Boltzmann constant, T is the local temperature, $Z * e$ is the effective ion charge, j is thelocal current density, ρ is the electrical resistivity which is dependent on temperature given as $\rho = \rho_0(1+\alpha(T-T_0))$, α is the temperature coefficient of resistivity, ρ_0 is the electrical resistivity at temperature T_0, D_0 is the prefactor of the self-diffusion coefficient of the interconnect metal, EA is the activation energy for the self-diffusion of the interconnect metal, Q^* is the heat of transport of interconnect metal, Ω is the atomic volume ($\Omega = 1/N$) of the interconnect metal, σ_H is the local hydrostatic stress, and is calculated using the average of the hydrostatic stress values in the interconnect in the x, y, z direction as $\sigma_H = (\sigma_{xx} + \sigma_{yy} + \sigma_{zz})/3$.

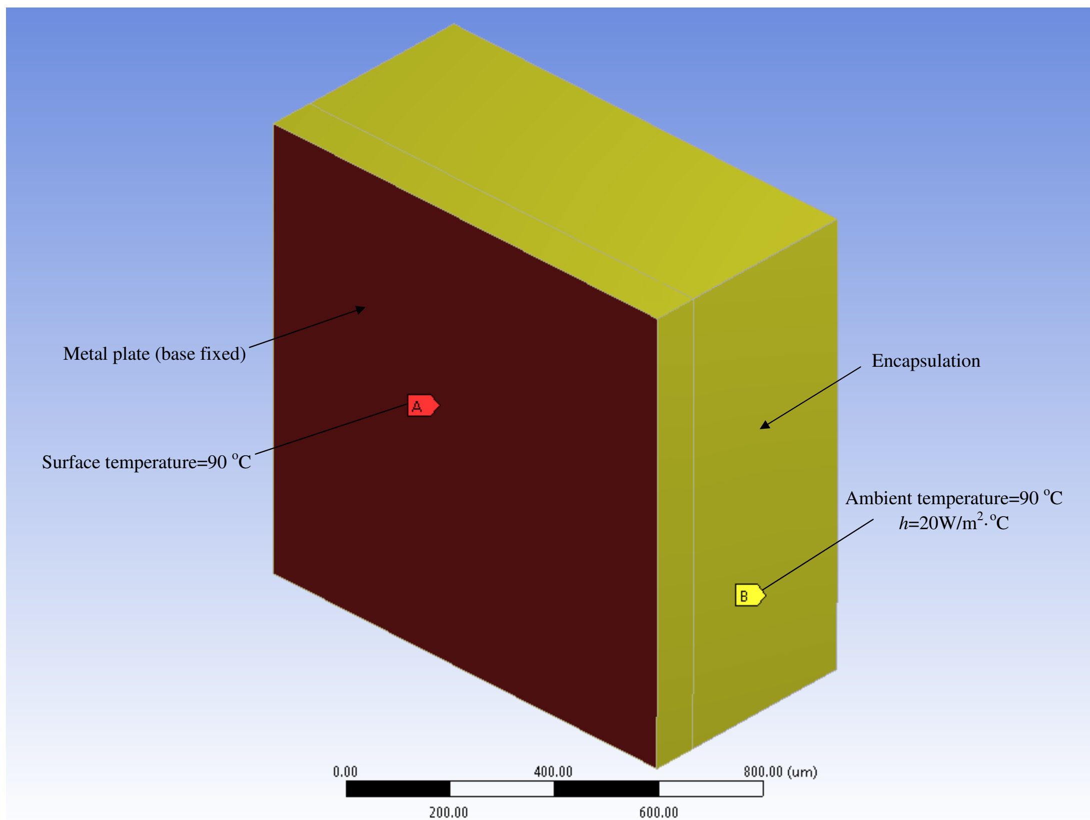

Fig. 5. The boundary conditions of the electro-thermo-structural simulation, titled view from the back[37]

After obtaining the atomic fluxes, the divergences due to the three driving forces are computed using Eqs. (4) ~ (6) respectively[10],

$$div(\overrightarrow{J_{EWF}}) = (\frac{E_A}{k_B T^2} - \frac{1}{T} + \alpha\frac{\rho_0}{\rho}) \cdot \overrightarrow{J_{EWF}}\, gradT, \tag{4}$$

$$div(\overrightarrow{J_T}) = (\frac{E_A}{k_B T^2} - \frac{3}{T} + \alpha\frac{\rho_0}{\rho}) \cdot \overrightarrow{J_T}\, gradT + \frac{NQ^* D_0}{3k_B^3 T^3} j^2\rho^2 e^2 \exp(-\frac{E_A}{k_B T}), \tag{5}$$

$$\begin{aligned} div(\overrightarrow{J_S}) = (\tfrac{E_A}{k_B T^2} - \tfrac{1}{T}) \cdot \overrightarrow{J_S}\, gradT + \tfrac{2EN\Omega D_0\alpha_1}{3(1-\nu)k_B T} \exp(-\tfrac{E_A}{k_B T})(\tfrac{1}{T} - \alpha\tfrac{\rho_0}{\rho}) grad^2 T \\ + \tfrac{2EN\Omega D_0\alpha_1}{3(1-\nu)k_B T} \exp(-\tfrac{E_A}{k_B T}) \tfrac{j^2\rho^2 e^2}{3k_B^2 T} \end{aligned} \tag{6}$$

where E, α_1 and v are the Young's Modulus, thermal expansion coefficient, and Poisson ratio of the interconnect metal. The details of the finite element formulation of the above variation problem can be found in [38].

After performing the electro-thermo-structural simulation, the current density, temperature, temperature gradient, and thermo-mechanical stress gradient of the interconnects are extracted and used to compute the AFDs based on Eqs. (1) $\sim$ (6). The flowchart for the computation of the AFDs is shown in Fig. 6. The total AFD in the interconnects is the sum of the three AFDs from their respective driving forces.

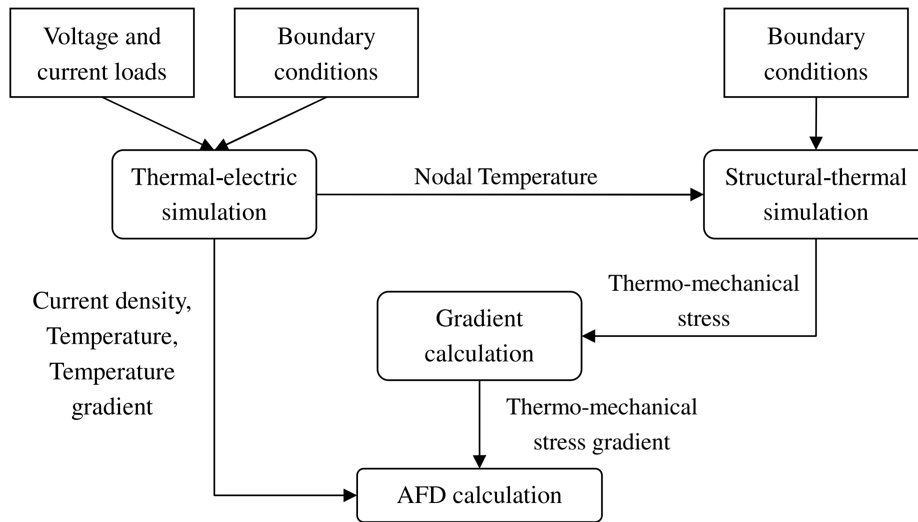

Fig. 6. The flowchart for the computation of the atomic flux divergences[16]

4 Results and discussions

The total AFD distribution and the maximum total AFD of Structures (a) to (k) are shown in Fig. 7 and summarized in Tab. 4. In Fig. 7, the arrows indicate the maximum AFD location.

The observed summaries shown in Tab. 4 may be explained as follows:

Under the circuit operation condition, the AFD due to the thermo-mechanical stress gradient induced driving force (AFD_S) has more than 90% contribution to the total AFD among the three driving forces[17]. The total AFD distribution and the location of the maximum total AFD of the 3D model are mainly determined by that of the AFD_S. Under this condition, the effect due to the thermo-mechanical stress gradient and the temperature gradient dominate over that due to the current density in the calculation of the AFD_S. The location of the maximum AFD_S is found at the place where the product of the thermo-mechanical stress gradient and the temperature gradient is the highest[17], and it is the location of the maximum total AFD, as indicated by the red arrows in Fig. 7.

As the path of the main current, the temperature at the PMOS region is higher than that at the NMOS region. High temperature is found at the region between the PMOS contacts and the vias due to the high

Table 4. Maximum total AFD of the different structures

Structural changes	Maximum total AFD (atoms/μm^3·s)			Remarks
Distance between the vias and the contacts	1.5 μ m (Fig. 7(a)) 1.71×10^8	1μ m (Fig. 7(b)) 1.52×10^8	0μ m (Fig. 7(c)) 1.09×10^8	The closer the vias to the contacts, the smaller the max AFD
Inter-transistor distance	2μm (Fig. 7(d)) 1.09×10^8	5μm (Fig. 7(e)) 1.04×10^8	8μm (Fig. 7(f)) 1.04×10^8	Insignificant effect
Number and position of the contacts	6 (Fig. 7(d)) 1.09×10^8	3 near to via (Fig. 7(g)) 1.36×10^8	3 far from via (Fig. 7(h)) 1.72×10^8	Fewer contacts increase the max AFD, especially when the distance between the contacts and the vias is larger
Metal structure at the output line	Metal 1+2 (Fig. 7(d)) 1.09×10^8	Metal 1 only (Fig. 7(i)) 1.59×10^7		Metal 1 only structure shows lower max AFD and an even total AFD distribution
Number and position of the metal layers	2 (Fig. 7(d)) 1.09×10^8	6 directly above Metal 2 (Fig. 7(j)) 1.54×10^8	6 5μm away (Fig. 7(k)) 1.36×10^8	Higher number of metal layers increases the max AFD. The increase in max AFD is smaller when the additional metal layers are added further away from the transistor

current density at that location. However, this temperature rise is much smaller as compared with the difference between the test temperature of 90ºC and the stress free temperature of the Cu interconnects which is assumed as 350ºC[24, 33]. The thermo-mechanical stress of the model is therefore mainly determined by the intrinsic stress of the interconnects. The values and distributions of the thermo-mechanical stresses and stress gradients of Structures (a) to (k) are similar due to their similar intrinsic stresses. The values and locations of the maximum AFD_S and the total AFD of these structures are therefore mainly affected by the temperature gradient of the model. The temperature gradient profile at the location with the maximum total AFD of the different interconnect structures is shown in Fig. 8, and it shows a similar trend as the values of the maximum total AFD in Tab. 4.

Discussion of the values and locations of the maximum total AFD of different interconnect structures in Categories (I) to (V) shown in Section 2 are as follows:

(I) From Fig. 9(a), we can see that there are two current crowding places for Structure(a), the Metal 1/Via 12 interface (Site A) and the contact/Metal 1 interface (Site B). As can be seen in Fig. 9(a) and Fig. 10(a), though the current density at Site A is higher than that at Site B, the temperature gradient at Site A is much smaller than at Site B due to the relatively uniform temperature distribution at Site A as a result of high current crowding. The temperature gradient is higher at the bottom of the PMOS contacts, which is closer to both the heat source (the diffusion region) and the heat sink (the base of the metal plate). The current density and the temperature of the PMOS contacts gradually decrease at the region away from Site A and B, and the temperature gradient follows this trend. The location of the maximum total AFD of Structure (a) is found at the contact/Metal 1 interface (Site B) with the highest value of the product of the thermo-mechanical stress gradient and the temperature gradient.

The change in the position of the vias causes a change in the value and distribution of the current density as shown in Fig. 9(b) and Fig. 9(c). When the distance between the vias and the contacts decreases, the crowding effect reduces. This results in a lower current density with a smaller via/contact distance, especially when the vias are directly above the contacts. The reduction in the current density causes a lower heat up and a smaller temperature gradient as shown in Fig. 8, and thus Structures (b) and (c) have smaller maximum AFD_S and total AFD as compared with Structure (a). A smaller maximum total AFD means a longer void nucleation time. As the void nucleation time occupies a large portion of the EM lifetime[19], increasing the

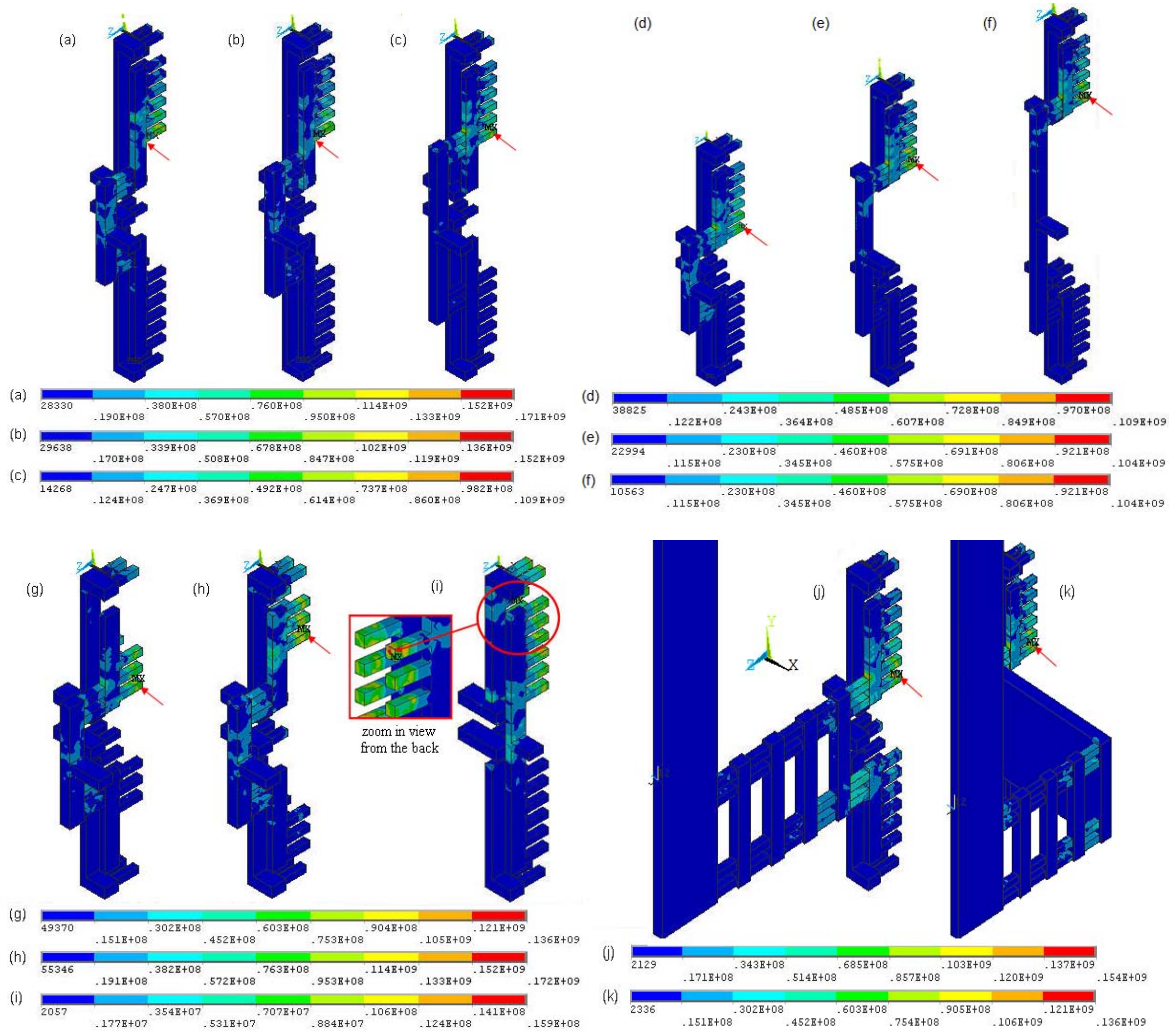

Fig. 7. The total AFD distributions of Structures (a) to (k) (unit: atoms/$\mu m^3 \cdot s$)

void nucleation time can effectively enhance the EM lifetime of the circuit. Structure (b) and (c) are expected to have a longer EM lifetime than Structure (a).

Structure (b) has the same location of the maximum total AFD (Site B) as Structure (a). For Structure (c), the contact/Metal 1 interface (Site B) is no longer a high current crowding region when the vias are directly above the contacts, and thus the temperature gradient at this location decreases significantly as shown in Fig. 10(c). The location of the maximum AFD_S and total AFD changes to the bottom of the contact (Site C) where the product of the stress gradient and the temperature gradient is the highest. Besides the effect due to current crowding, the temperature gradient at Site A increases as the vias are now directly above the heat source (the diffusion region) and the heat sink (the metal plate base). The location of the 2nd highest AFD_S and total AFD is found at Site A.

(II) The increase in the inter-transistor distance from 2 μm to 5 μm causes a 0.10% reduction in the circuit temperature and temperature gradient as the heat sources are further apart. The reduction in the temperature and the temperature gradient gives rise to a 4.59% reduction in the value of the maximum total AFD (i.e. 4.81% improvement in the EM lifetime). The distributions of the total AFD and the temperature gradient, the locations of the maximum total AFD for Structures (d) and (e) are similar to (c) due to their similar structures. As the amount of current flow in the NMOS is more than 10 times smaller than in the PMOS, this circuit has only one main heat generating transistor. The effect of the inter-transistor distance is insignificant and separating the two transistors further apart has very limited impact on the circuit temperature and temperature

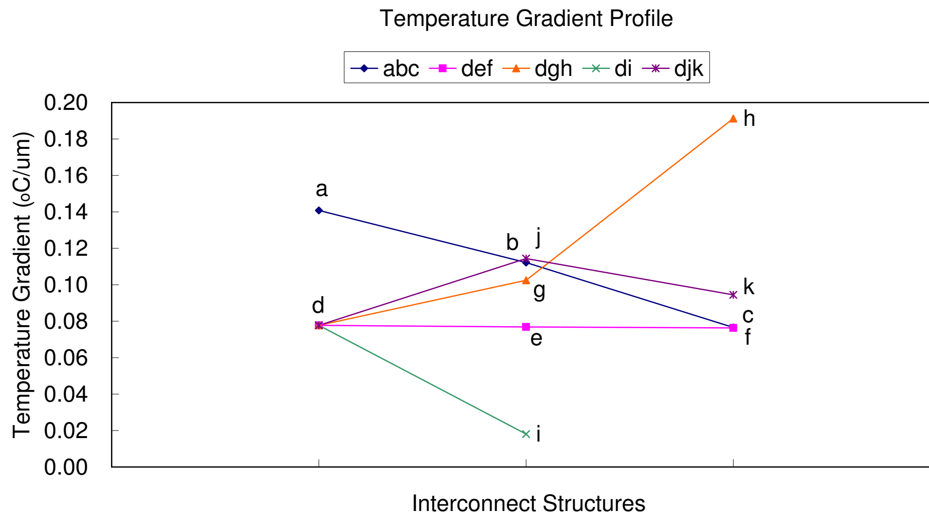

Fig. 8. The temperature gradient profile of the different interconnect structures

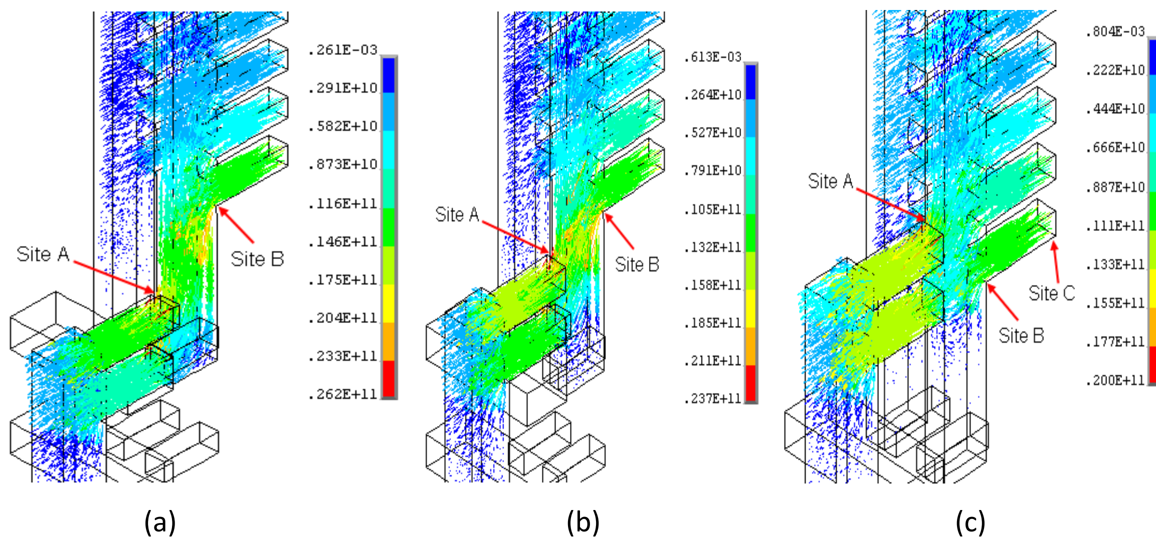

Fig. 9. Vector plot of the current density distributions of Structures (a) to (c) (unit: pA/μm2)

gradient. No further reduction in the value of the maximum total AFD is observed when the inter-transistor distance increases from 5 μm to 8 μm.

(III) When the number of contacts is reduced from 6 to 3, the increase in current density at each contact causes a rise in the circuit temperature and temperature gradient[27]. 24.77% and 57.80% rise in the values of the maximum total AFD are observed for Structures (g) and (h) (i.e. the 3 contacts structure) respectively as compared with Structure (d) (i.e. the 6 contacts structure), implying a shorter void nucleation time with fewer contacts. Structure (g) and (h) are expected to have 32.92% and 136.97% reduction in the EM lifetime respectively as compared with Structure (d). This result agrees with the reported experimental observations in [20, 22]. Structure (h) has an even higher maximum total AFD than (g) due to the change in the position of the contacts (i.e. further away from the vias), which corresponds to the observations in (I). The location of the maximum AFD for Structure (h) is different from Structure (a) as the increase in the temperature gradient at the contact bottom has a larger impact on the AFD_SM than the increase in the current density at the contact/Metal 1 interface. The locations of the maximum AFD_SM and the maximum total AFD are found at the contact bottom.

(IV) In the previous structures, the total AFD is always higher at the contacts nearer to the current crowding site (i.e. nearer to the vias at the output line), and lower at the contacts further away. When Metal 1 is used as

the output line, the removal of the Metal 2/Via 12 structure eliminates the current crowding at this location. The current density and temperature gradient distributions of each contact become more uniform. Hence a uniform distribution of the total AFD is obtained. The avoidance of the current crowding results in an 85.41% reduction in the maximum total AFD and a 585.40% increase in the EM lifetime for Structure (i) as compared with Structure (d). The location of the maximum total AFD is found at the contact connecting to the source interconnects where the voltage is higher than at the drain interconnects (3.30 V and 1.30 V respectively).

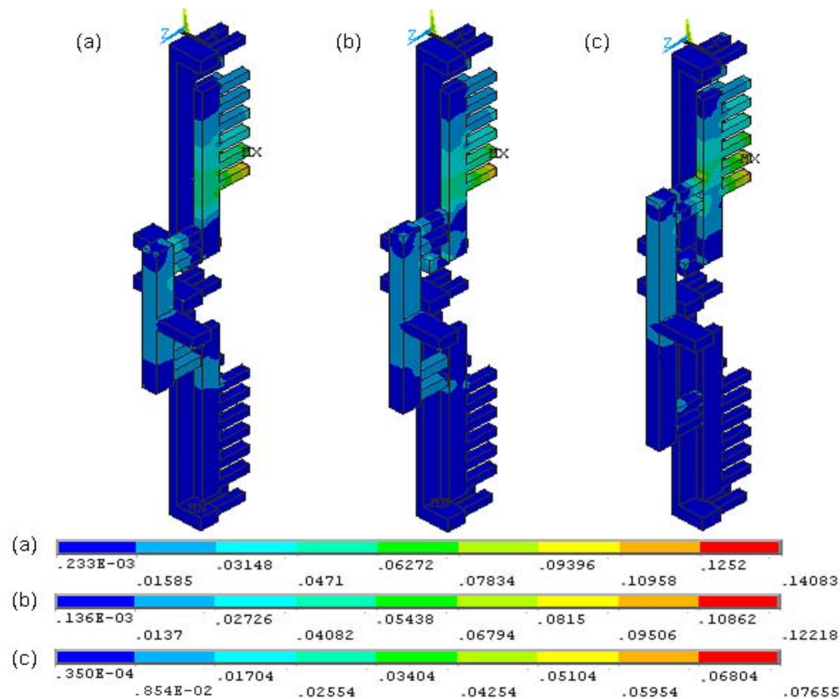

Fig. 10. Temperature gradient distributions of Structures (a) to (c) (unit: oC/μm)

(V) Adding more metal/via layers causes an increase in the temperature gradient in the z-axis direction due to a larger distance from the top metal to the heat source, and thus the maximum total AFD for this structure increases. The total AFD distribution and the location of the maximum total AFD for Structure (j) is almost the same as Structure (d), therefore the trends in (I) to (III) (where only 2 metal layers are considered) apply to the structures up to 6 metal layers. When the metal/via stacks are added at a distance away from the transistor (i.e. away from the heat source), the impact of the additional metal/via layers on the temperature gradient of the circuit reduces. This results in a smaller increase in the maximum total AFD for Structure (k) (24.77%) as compared with (j) (41.28%). 32.92% and 70.30%. reduction in the EM lifetime are observed for Structure (k) and (j) respectively as compared with Structure (d). The maximum total AFD further reduces to 1.30×108 atoms/$\mu m^3 \cdot s$ when the width of Metal 2 to 6 is doubled, and this is due to the decrease in current density with wider metal lines and more vias.

From the above observations, it is clear that we can improve the EM lifetime of the circuit by placing the vias directly above the contact region, using more contacts and more uniform interconnect structures (e.g. use Metal 1 as the output line instead of the metal/via stacks), or adding the Metal 3 to Metal 6 connection away from the transistors.

5 Conclusions

The line-via structure simulation may not always be able to represent the actual void nucleation location of the circuit under the circuit operation condition. These drive the need for the complete 3D modelling at

the circuit level. The traditional 3D EM modelling for the study of the interconnect structures are all using the line-via structure. These partial-circuit modelling may overlook some factors affecting the circuit EM reliability. In this paper, a few sets of 3D models were constructed at the circuit level based on the output stage of a class-AB amplifier, and the differences in their maximum total AFD were compared.

Higher maximum total AFD were observed for structures with a larger via/contact distance, a shorter inter-transistor distance, fewer contacts, non-uniform metal structures, and more metal layers. Some changes in structure cause a change in maximum total AFD location. Some of the observations were in agreement with the available literature reports in [20, 22] and thus the 3D circuit model can be used to exam the impact of the structural modifications of the interconnects on the circuit EM lifetime. Modifications can be made to the layout designs based on the simulation results so as to improve the EM lifetime of the circuit.

Due to the complexity of the model and the constraint in computation memory, the microstructure and back stress effects are not included in the model. The dynamic simulation of the void nucleation of the 3D circuit model with the consideration of the microstructure and back stress effects is an area for further study. Integrating the Neural Network method[44] into the model to speed up the computation is another area of future research, so that the application to the large and complex circuits will become possible.

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