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A new Space-Vector Pulse Width Modulation Algorithm for multilevel inverters

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Abstract. This paper proposed a new Space Vector Pulse Width Modulation (SVPWM) algorithm for multi-level neutral point clamped inverter. The SVPWM method is an advanced, computation intensive PWM method and is also possibly the best among all the PWM techniques for variable frequency drive applications. The SVPWM involves the sector identification, determination of switching voltage vectors, switching vector sequence and dwelling time calculations. But as the level of the inverter increases, the sector identification, switching vector determination and dwelling time calculation becomes more complex. The computational complexity and execution time increases. In the proposed method, a correction to the duty cycles of reference vector is applied to easily identify the location of reference vector in each region of multi-level inverter. Then the appropriate switching sequence of the identified region and calculation of switching times for each state with the obtained duty cycles are estimated. The scheme can be extended to high-level inverters. Based on the above method the simulation results have been presented and analyzed for six-level and seven-level neutral point clamped inverters. The total harmonic distortion have been calculated and compared with lower levels also. The results have been good agreement with the published work.

Keywords: multi-level inverters, SVPWM, neutral point clamped inverter, induction motor, THD

1 Introduction

Multilevel Inverter technology finds significant applications in the area of high-power medium-voltage energy control. Multilevel inverters generate sinusoidal voltages from discrete voltage levels and pulse width modulation strategies accomplish this task of generating sinusoids of variable voltage and frequencies. The two main techniques of PWM generation for multilevel inverters are Sine-triangle PWM and Space Vector PWM. SVPWM involves synthesizing the reference voltage space vector by switching among the three nearest voltage space vectors[14]. Space Vector PWM is considered a better technique of PWM implementation owing to its associated advantages of (1) Better fundamental output voltage. (2) Better harmonic performance. (3) Easy implementation in Digital Signal Processor and Microcontrollers. The implementation of SVPWM involves (1) Identification of the sector in which the tip of the reference vector lies. (2) Determination of the three nearest voltage space vectors. (3) Determination of the duration of each of these switching voltage space vectors and (4) Choosing an optimized switching sequence. The sector identification can be done by using coordinate transformation of the reference vector into a two dimensional coordinate system. The sector can also be determined by resolving the reference phase vector along a, b and c axis and by repeated comparison with discrete phase voltages. After identifying the sector, the voltage vectors at the vertices of the sector are to be determined. Once the switching voltage space vectors are determined the switching sequences can be identified using lookup tables[6]. The calculations of the duration of the voltage vectors can be simplified by

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mapping the identified sector correspond to a sector of two-level inverter. To obtain optimum switching, the voltage vectors are to be switched for their respective durations, in a sequence such that only one switching occurs as the inverter moves from one switching state to another[9, 15, 17].

But as the level of the inverter increases, the sector identification, switching vector determination and dwelling time calculation becomes more complex. The computational complexity and execution time increases[8]. The duty cycles of reference voltage vector will be m_1, m_2 and $1-(m_1+m_2)$. The values of m_1 and m_2 are useful in identifying the region where reference vector is located, which is the major problem in case of multi-level inverters. In this paper, a correction to the duty cycles of reference vector is applied to easily identify the location of reference vector in each region of multi-level inverter. Then the appropriate switching sequence of the identified region and calculation of switching times for each state with the obtained duty cycles are estimated. This new SVPWM algorithm can be extended to higher level inverters also.

2 Neutral point clamped multilevel inverters

In these inverters, the voltage across semiconductor switches is limited by diodes connected to various DC levels as such it is called Diode Clamed Multilevel inverters. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors addition across source dc-bus. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology Neutral Point Clamped (NPC) inverter was introduced. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three- level. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications. The functional diagram of an n-level NPC inverter utilizing single-pole n-throw switches is shown in Fig. 1. To result a defined output voltage, $(n-1)$ consecutive switches of each leg must be in the

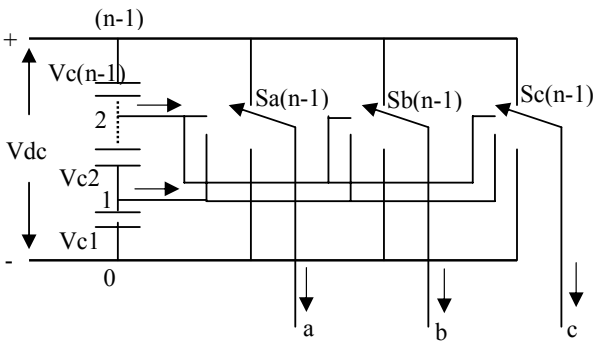


Fig. 1. Functional diagram of n-level NPC inverter

On-state. All possible combinations of the above functional diagram can be summarized by the Eq. (1).

$$\sum_{j=1}^{n} S_{ij} = 1 \text{ with } i = \{a, b, c\}. \tag{1}$$

The variables S_{ij} are the control functions of the single-pole n-throw switches. These variables define the position of switches, so that they have the unity value when the i output is connected to j point; other wise they are zero. Referring all of the voltages to the lower DC-link voltage level ("0" reference) each output voltage consists of contributions by a determined number of consecutive capacitors:

$$V_{i0} = \sum_{j=1}^{n} \left(S_{ij} \sum_{p=1}^{j} Vc_p \right) \text{ with } i = \{a, b, c\}. \tag{2}$$

When balanced distribution of DC-link voltage among the capacitors is assumed:

$$V_{i0} = \frac{Vdc}{n-1} \sum_{j=1}^{n} jS_{ij} \quad \text{with} \quad i = \{a, b, c\}. \tag{3}$$

In 1980s, three-level NPC inverter is most practical and widely studied multilevel inverter topology. One application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line. Another application would be as a variable speed drive for high-power medium-voltage ($2.4\ kV$ to $13.8\ kV$) motor.

The advantages of NPC inverter are:

(1) All of the phases share a common dc bus, which minimizes the capacitance requirements of the inverter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive. (2) The capacitors can be pre-charged as a group. (3) Efficiency is high for fundamental frequency switching.

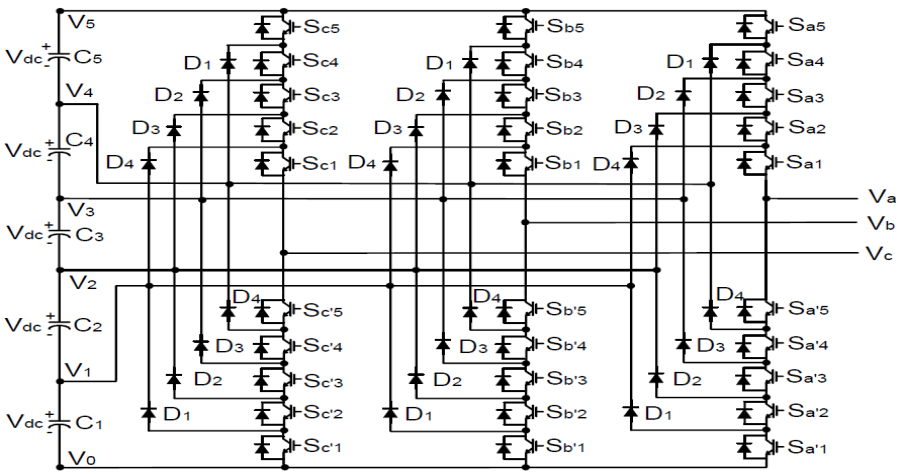


Fig. 2. Functional diagram of six-level NPC inverter

The six-level neutral point clamped inverter is as shown in Fig. 2. But in case of seven-level inverters six switches from each phase-leg will be ON at any point of time to produce predetermined output at phases. The possible switching combinations will be 343.

3 Space Vector Pulse Width Modulation for multi-level inverters

Space Vector PWM (SVPWM) is quite different from other PWM techniques. With other PWM techniques, the inverter can be thought of as three separate stages, which create each phase wave form separately. However, the SVPWM treats inverter as a single unit with inverter in specific unique state[6]. Modulation is achieved by switching the state of the inverter. SVPWM is a digital modulating technique where the objective is to generate PWM load line voltages that are in average equal to given (or reference) load line voltages. This is done in each sampling period by properly selecting the switching states of the inverter and the calculation of the appropriate time period for each state. The SVPWM is advanced and, computation-intensive PWM method.

The space vector (V_s) constituted by the pole voltages of inverter V_{az}, V_{bz} and V_{cz} with 120° phase displacement can be defined as:

$$V_s = V_{az} + V_{bz} \exp[j(2\pi/3)] + V_{cz} \exp[\mathrm{j}(4\pi/3)]. \tag{4}$$

The space vector, V_s can be resolved into two rectangular components namely V_α and V_β as indicated below:

Table 1. General characteristics of multi-level inverters

NPC inverter	a	b	c	d	e	f	g
n-level	$6(n-1)$	$(n-1)$	n^3	$n^3-(n-1)^3$	$(n-1)^3$	$2n-1$	$4n-3$
2-level	6	1	8	7	1	3	5
3-level	12	2	27	19	8	5	9
4-level	18	3	64	37	27	7	13
5-level	24	4	125	61	64	9	17
6-level	30	5	216	91	125	11	21
7-level	36	6	343	127	216	13	25

a : number of switches with free wheeling diodes

a : number of consecutive switches of each leg to be in ON-state

b : number of different voltage states of the inverter

c : number of switches with free wheeling diodes

d : number of unique voltage states of the inverter

e : number of redundant voltage states of the inverter

g : phase voltage levels

$$V_s = V_\alpha + \mathrm{j}V_\beta, \tag{5}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \tag{6}$$

Equating volt-seconds along α axis gives:

$$V_s \cos\alpha \times T_s = V_{dc} \times T_1 + (V_{dc}\cos 60^\circ) \times T_2. \tag{7}$$

Equating volt-seconds along β axis gives:

$$V_s \sin\alpha \times T_s = (V_{dc}\sin 60^\circ) \times T_2. \tag{8}$$

Solving Eq. (7) and Eq. (8) gives the values for the on-time periods T_1, T_2 and T_0 are

$$T_1 = \frac{V_s \times T_s \times \sin(\pi/3-\alpha)}{V_{dc} \times \sin(\pi/3)}, \quad T_2 = \frac{V_s \times T_2 \times \sin\alpha}{V_{dc} \times \sin(\pi/3)}, \quad T_0 = T_s - (T_1 + T_2). \tag{9}$$

In multilevel inverters the reference voltage vector can be reproduced in the average sense by switching amongst the inverter states situated at the vertices, which are in closest proximity to it. In case of two-level inverter, the identification of reference vector location in a Sector is straight forward. However, in higher level inverter, the existence of more than one number of regions in Sector will require additional mathematical computation to identify the region where the reference vector is located. The duty cycles (ON time for each state) will be found by equating volt-seconds of reference voltage with nearest three states.

$$m = d_1V_1 + d_2V_2 + d_3V_3, \tag{10}$$

where d_1, d_2 and d_3 are duty cycles of nearest voltage vectors V_1, V_2 and V_3 and 'm' is the voltage reference vector.

Calculation of duty cycles:

The vector states at vertices of each region can be identified from space vector diagrams. Consider the space vector diagram of Sector 1 of Seven-level inverter, shown in Fig. 3. The reference vector m_3 is located in region 2 of three-level inverter. The m_6 and m_7 are reference vectors located in region 21 of six-level inverter and region 29 of seven- level inverter, respectively. m_{x1} and m_{x2} ($x = 3$ or 6 or 7) are projections of reference

vectors on to zero and sixty degrees axes (angle 'θ' is angle made by reference vector from zero axes i.e., starting of sector 1; be noted m_3, m_6 and m_7 are having different angle 'θ' value). The reference vector can be synthesized by sequential switching operation of nearest three switching states (vertices of the region in which reference vector is located). The lengths of new vectors can be found from the below equation:

$$m_1 = m \times (\cos\theta - \sin\theta/\sqrt{3}) \quad m_2 = 2 \times m \times (\sin\theta/\sqrt{3}). \tag{11}$$

The values of m_1 and m_2 for reference vector in each region can be calculated with Eq. (11). The duty cycles of vertices of reference voltage will be m_1, m_2 and $[1-(m_1+m_2)]$. For example, with reference to m_3 (reference vector in region 2), the reference vector can be synthesized by switching vectors V_1, V_2 and V_3. It shall be important to note that duty cycle for switching state V_1 shall be length of the vector joining V_3 and V_1, whereas, m_1 is the projection of reference vector m_3 from origin. As such, the corrected duty cycle for switching state V_1 in present case would be $(m_1 - 0.25)$. The length of vector joining V_3 and V_2 is m_2. As such, corrected duty cycles for switching states V_1, V_2 and V_3 would be $(m_1 - 0.25)$, m_2 and $(0.75 - m_1 - m_2)$ respectively.

The values of m_1 and m_2 are useful in identifying the region where reference vector is located, which is the major problem in multilevel inverters. The conditions for identifying reference vector location in each region and the corrected duty cycles for each of the level of inverter are shown in Tab. 2. Once the region is identified, the appropriate switching sequence of a region can be identified.

The ON time period for each state can be calculated with duty cycles obtained:

$$T_{\text{ON}} \text{ for state 1} = T_s \times m_1, \quad T_{\text{ON}} \text{ for state 2} = T_s \times m_2, \quad T_{\text{ON}} \text{ for state 3} = T_s \times [1-(m_1+m_2)]. \tag{12}$$

The SVPWM algorithm for multilevel inverters:
(1) Find the sector in which V_{ref} lies.
(2) Calculate m_1, m_2 from Eq. (11) and compute $(m_1 + m_2)$ of reference voltage.
(3) Find the region in which V_{ref} is located.
(4) Identify the nearest three vectors (vertices of region) to the V_{ref}.
(5) Select appropriate switching sequences.
(6) Compute ON time for each switching state.
(7) Place the inverter states in the respective states for the calculated ON times.

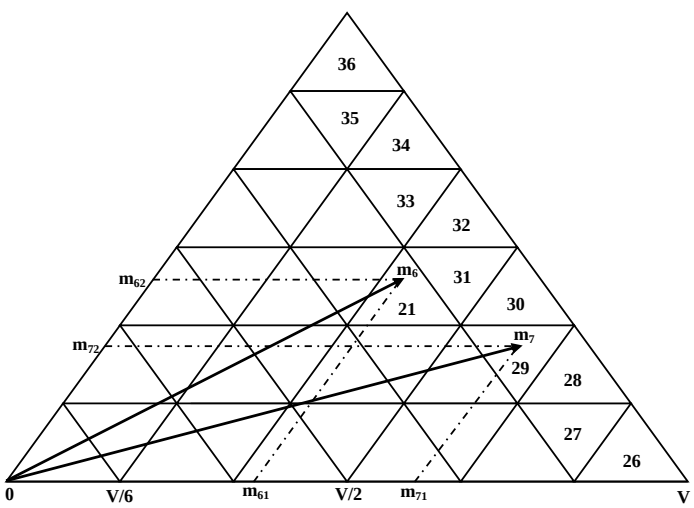
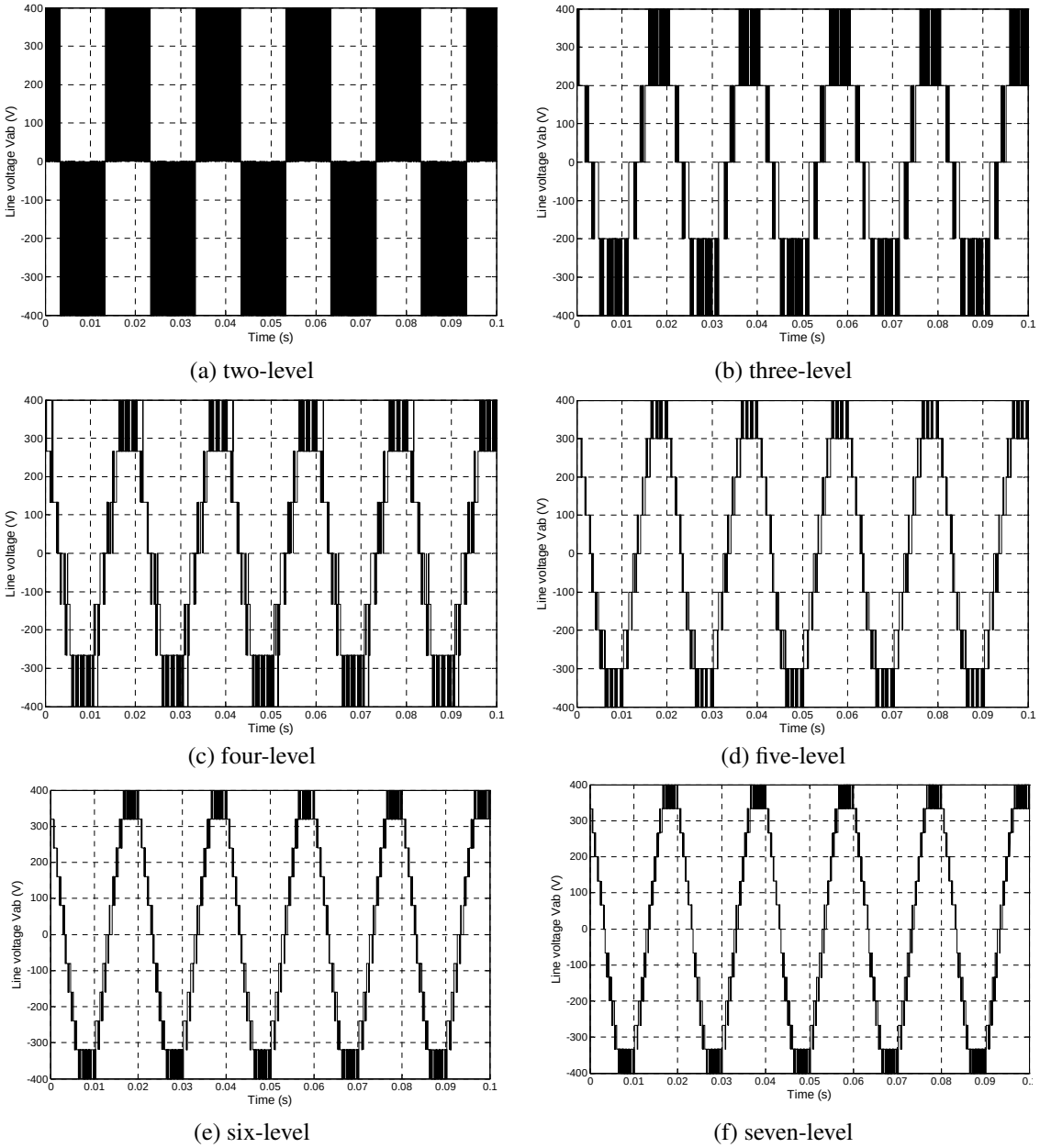


Fig. 3. First sector of seven-level inverter space vector diagram



(a) two-level (b) three-level

(c) four-level (d) five-level

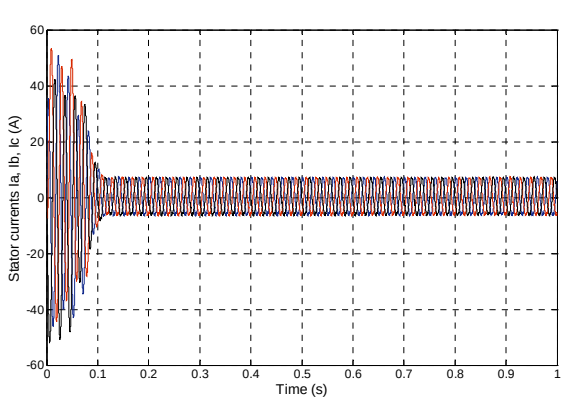
(e) six-level (f) seven-level

Fig. 4. The line to line voltage of multi-level inverter

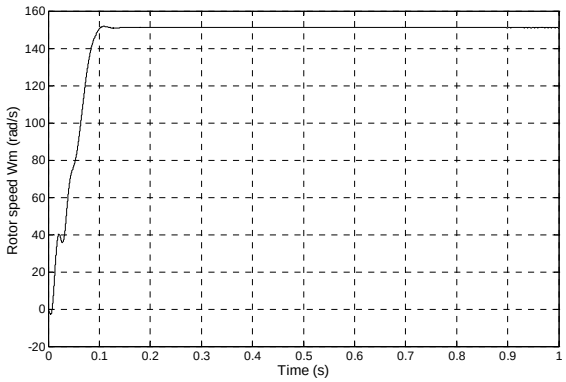
4 Simulation results and discussion

The simulation is carried out for the Two-level, Three-level, Four-level, Five-level, Six-level and Seven-level inverters using the new Space vector PWM technique and the simulation results are presented. Fig. 4 shows that the generated line to line voltage is very much improved with the level of inverter. Fig. 5 shows the stator current, torque and speed of seven-level inverter fed induction motor and Fig. 6 shows the total harmonic distortion (THD), which is highly reduced as the level of inverter increases. From the results it is observed that the generated voltage spectrum is very much increased with the level of inverter. The THD values of the proposed inverter are lower than that of the same inverter using other modulation techniques. The improved speed and torque characteristics are obtained with this algorithm. The torque ripples are also reduced and output voltage waveform is highly improved. The fundamental component of the output voltage is increased with the level of inverter.

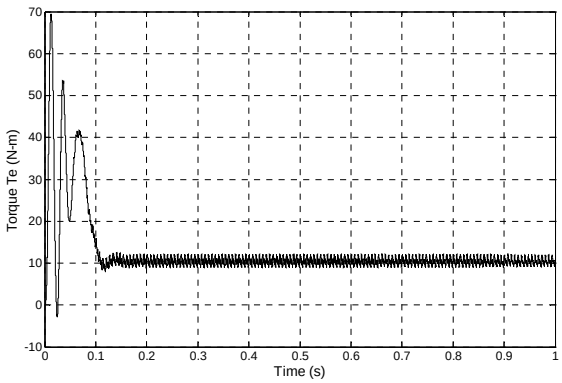
The simulation is carried out for the two-level, three-level, four-level, five-level, fix-level and feven-level inverters using the new space vector PWM technique with the following parameters.



(a) Stator currents



(b) Speed



(c) Torque

Fig. 5. Stator current, speed and torque of seven-level inverter fed induction motor

Table 2. Location of reference vector in seven-level inverter

Region	Condition for location of reference vector	Corrected m_1, m_2 and m_3 for switching states	Region	Condition for location of reference vector	Corrected m_1, m_2 and m_3 for switching states
	$0.834 < m_1 < 1$;	$m_1 = m_1 - 0.833$;		$0.333 < m_1 < 0.5$;	$m_1 = m_1 - 0.333$;
26	$m_2 < 0.167$;	$m_2 = m_2$;	32	$0.5 < m_2 < 0.667$;	$m_2 = m_2 - 0.5$;
	$(m_1 + m_2) < 1$;	$m_3 = 1 - m_1 - m_2$;		$(m_1 + m_2) < 1$;	$m_3 = 1 - m_1 - m_2$;
	$0.667 < m_1 < 0.834$;	$m_1 = 0.833 - m_1$;		$0.167 < m_1 < 0.333$;	$m_1 = 0.5 - m_1$;
27	$m_2 < 0.167$;	$m_2 = 0.167 - m_2$;	33	$0.5 < m_2 < 0.667$;	$m_2 = 0.667 - m_2$;
	$(m_1 + m_2) > 0.834$;	$m_3 = m_1 + m_2 - 0.834$;		$(m_1 + m_2) > 0.834$;	$m_3 = m_1 + m_2 - 0.834$;
	$0.667 < m_1 < 0.834$;	$m_1 = m_1 - 0.667$;		$0.167 < m_1 < 0.333$;	$m_1 = m_1 - 0.167$;
28	$0.167 < m_2 < 0.333$;	$m_2 = m_2 - 0.167$;	34	$0.667 < m_2 < 0.834$;	$m_2 = m_2 - 0.667$;
	$(m_1 + m_2) < 1$;	$m_3 = 1 - m_1 - m_2$;		$(m_1 + m_2) < 1$;	$m_3 = 1 - m_1 - m_2$;
	$0.5 < m_1 < 0.667$;	$m_1 = 0.667 - m_1$;		$m_1 < 0.167$;	$m_1 = 0.167 - m_1$;
29	$0.167 < m_2 < 0.333$;	$m_2 = 0.333 - m_2$;	35	$0.667 < m_2 < 0.834$;	$m_2 = 0.834 - m_2$;
	$(m_1 + m_2) > 0.834$;	$m_3 = m_1 + m_2 - 0.834$;		$(m_1 + m_2) > 0.834$;	$m_3 = m_1 + m_2 - 0.834$;
	$0.5 < m_1 < 0.667$;	$m_1 = m_1 - 0.5$;		$m_1 < 0.167$;	$m_1 = m_1$;
30	$0.333 < m_2 < 0.5$;	$m_2 = m_2 - 0.333$;	36	$0.834 < m_2 < 1$;	$m_2 = m_2 - 0.834$;
	$(m_1 + m_2) < 1$;	$m_3 = 1 - m_1 - m_2$;		$(m_1 + m_2) < 1$;	$m_3 = 1 - m_1 - m_2$;
	$0.333 < m_1 < 0.5$;	$m_1 = 0.5 - m_1$;			
31	$0.333 < m_2 < 0.5$;	$m_2 = 0.5 - m_2$;			
	$(m_1 + m_2) > 0.834$;	$m_3 = m_1 + m_2 - 0.834$;			

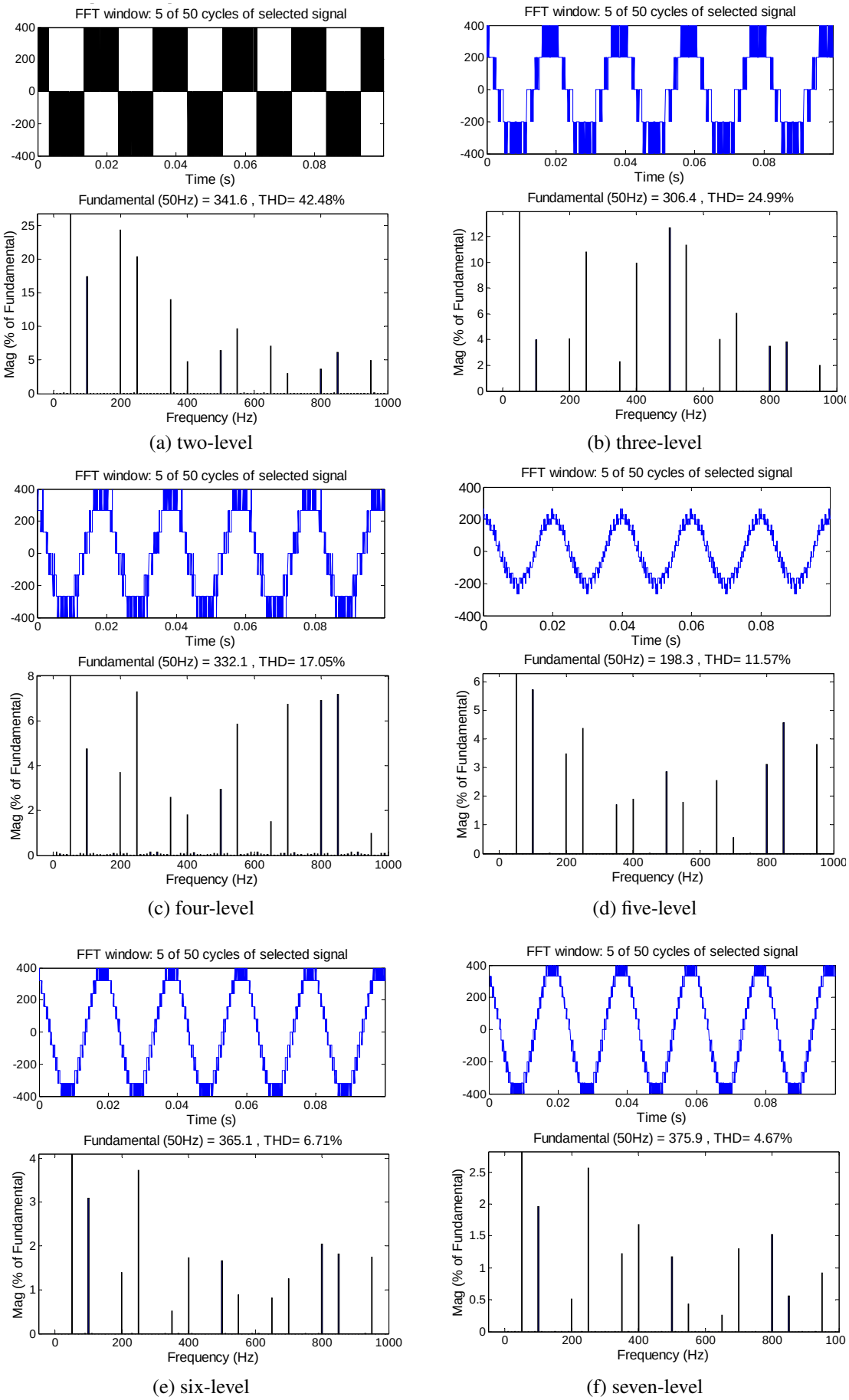


Fig. 6. FFT analysis and total harmonic distortion (THD) for multi-level inverters

Table 3. Switching sequence for seven-level inverter

Sector	Region	ON Sequence	Sector	Region	ON Sequence
1	26	500 600 610 611	2	47	050 060 160 161
	27	500 510 610 611		46	050 150 160 161
	28	510 610 620 621		45	150 160 260 261
	29	510 520 620 621		44	150 250 260 261
	30	520 620 630 631		43	250 260 360 361
	31	520 530 630 631		42	250 350 360 361
	32	530 630 640 641		41	350 360 460 461
	33	530 540 640 641		40	350 450 460 461
	34	540 640 650 651		39	450 460 560 561
	35	540 550 650 651		38	450 550 560 561
	36	550 650 660 661		37	550 560 660 661

Table 4. Simulation results with full-load on induction motor

Parameter	Inverter					
	2LI	3LI	4LI	5LI	6LI	7LI
No. of spikes/Half cycle in I - steady state	20	8	8	5	5	4
Peak to Peak I - starting	83	79	85	82	80	79
Peak to Peak I - steady state	15.4	16	14	12	11	10
Time taken to reach I - steady state	0.14	0.16	0.14	0.12	0.11	0.10
Speed ripple	0.3	0.2	0.2	0.5	0.3	0.1
THD	42.48%	24.99%	17.05%	11.57%	6.71%	4.67%

SVPWM parameters:
Modulation index $m = 0.866$; DC Supply voltage $= 400V$;
No. of switching intervals $= 192$; Sampling time $Ts = 1.984e - 5$ sec.
Induction Motor parameters:
2 HP, 1500 W, 400 V, 50 Hz, 4-pole, 1430 rpm, $R_s = 1.405\ \Omega$; $R_r = 1.395\ \Omega$; $L_s = 5.839\ mH$; $L_r = 5.839\ mH$; $L_m = 0.143\ H$; $J = 0.0131\ Kg - m^2$; $f_r = 0.002985\ N - m - s$.

5 Conclusion

In this paper a new space vector pulse width modulation (SVPWM) algorithm has been proposed and implemented for two-level, three-level, four-level, five-level, six-level and seven-level inverters. The SVPWM involves the sector identification, determination of switching voltage vectors, switching vector sequence and dwelling time calculations. But as the level of the inverter increases, the sector identification, switching vector determination and dwelling time calculation becomes more complex. The computational complexity and execution time increases. In the proposed method, a correction to the duty cycles of reference vector is applied to easily identify the location of reference vector in each region of multi-level inverter. Then the appropriate switching sequence of the identified region and calculation of switching times for each state with the obtained duty cycles are estimated. The scheme can be extended to high-level inverters also. Based on the reference vector correction, the simulation results have been presented and analyzed. It is observed that the generated voltage spectrum is very much improved with increase the level of inverter. The total harmonic distortion (THD) is highly reduced as the level of inverter is increases. The THD values of the proposed SVPWM algorithm for two-level, three-level, four-level, five-level, six-level and seven-level inverters are 42.48%, 24.99%, 17.05%, 11.57%, 6.71% and 4.67% respectively, which are lower than that of the same inverter using other modulation techniques. The results have been good agreement with the published work.

References

[1] T. Bruckner, D. Holmes. Optimal pulse-width modulation for three-level inverters. *IEEE Transactions on Power Electronics*, 2005, **1**(20): 82–89.

[2] S. Busquets-Monge, J. Bordonau, et al. The Nearest Three Virtual Space Vector PWM-A Modulation for the Comprehensive Neutral-Point Balancing in the Three-Level NPC Inverter. *IEEE Power Electronics Letters*, 2004, **2**(1): 11–15.

[3] K. Corzine. *Operation and design of multilevel inverters*. University of Missouri-Rolla, 2005. Technical Report.

[4] D. Holmes, T. Lipo. *Pulse Width Modulation for Power Converters-Principles and Practice*. New Jersey, IEEE Press, Wiley-Interscience.

[5] L. Hu, H. Wang, et al. A Simple SVPWM Algorithm for Multilevel Inverters. **in:** *35th Annual IEEE Power Electronics Specialist Conference*, Aachen, Germany, 2004.

[6] R. Kanchan, M. Baiju, et al. Space vector PWM signal generation for Multilevel Inverters using only sampled amplitudes of reference phase voltages. **in:** *IEE Proceedings*, *2*, vol. 152, 2005, 297–309.

[7] R. Kanchan, P. Tekwani, K. Gopakumar. Three-Level Inverter Scheme With Common Mode Voltage Elimination and DC Link Capacitor Voltage Balancing for an Open-End Winding Induction Motor Drive. *IEEE Transactions On Power Electronics*, 2006, **21**(6): 1767–1783.

[8] P. Kumar, J. Narasimham. A Novel PWM Scheme for Multilevel Voltage Source Inverter Fed Induction Motor. *International Journal of Applied Engineering Research*, 2009, **4**(5): 735–748.

[9] B. McGrath, D. Holmes, T. Lipo. Optimised Space Vector switching sequences for Multilevel inverters. *IEEE Transactions on Power Electronics*, 2003, **18**(6): 1293–1301.

[10] Z. Pan, F. Peng, et al. Voltage balancing control of diode-clamped multilevel inverter systems. *IEEE Transactions on Industry Applications*, 2005, **41**(6): 1698–1706.

[11] J. Pou, D. Boroyevich, R. Pindado. New Feed forward Space-Vector PWM Method to Obtain Balanced AC Output Voltages in a Three-Level Neutral-Point-Clamped Converter. *IEEE Transactions on Industrial Electronics*, 2002, **49**(5): 1026–1034.

[12] J. Rodriguez, J. Lai, F. Peng. Multilevel Inverters: A Survey of Topologies, Controls and Applications. *IEEE-IE Trans. On Industrial Electronics*, 2002, **49**(4): 724–738.

[13] M. Saeedifard, H. Nikkhajoei, R. Iravani. A Space Vector Modulated STATCOM Based on a Three-Level Neutral Point Clamped Converter. *IEEE Transactions On Power Delivery*, 2007, **22**(2): 1029–1039.

[14] P. Seixas, M. Mendes, et al. A Space Vector PWM Method for Three-Level Voltage Source Inverters. **in:** *IEEE Proceedings of Applied Power Electronics Conference and Exposition*, vol. 1, 2000, 549–555.

[15] J. Seo, C. Choi, D. Hyun. A new simplified space-vector PWM method for three level inverters. *IEEE Transactions on Power Electronics*, 2001, **16**(4): 545–550.

[16] R. Teichmann, S. Bernet. A Comparison of Three-Level Converters versus Two-Level Converters for Low-Voltage Drives, Traction, and Utility Applications. *IEEE Transaction on Industry Applications*, 2005, **41**(3): 855–865.

[17] S. Wei, B. Wu, Q. Wang. An improved space vector PWM control algorithm for multilevel inverters. **in:** *Proceedings of International Power Electronics and Motion Control Conference*, vol. 3, 2004, 1124–1129.